TANDY®

Service Manual

26-3814

PORTABLE DISK DRIVE 2

Catalog Number: 26-3814

CUSTOM MANUFACTURED FOR RADIO SHACK, A DIVISION OF TANDY CORPORATION

Portable Disk Drive 2 Service Manual

10 9 8 7 6 5 4 3 2 1

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1. INTRODUCTION

The Tandy Portable Disk Drive 2 is a stand-alone 3.5-inch, microfloppy disk drive. It interfaces to the portable computer through the RS-232C port and may be powered by batteries for maximum portability.

Its compactness and light weight enable it to be carried along with the portable computer. Although tiny in size, a 3.5-inch diskette can store up to 200,000 bytes of data.

2. GENERAL SPECIFICATIONS

1. Storage capacity (Formatted)
   - Per disk ..... 202.24K bytes
   - Per track ..... 2,560 bytes
   - Per hard sector ..... 1,280 bytes
2. Disk
   - Number of surfaces 1
   - Number of memory blocks 160
   - Total number of tracks 80
   - Total number of hard sectors 160
3. Recording systems
   - Recording method ..... FM
   - Recording density ..... 4,064 BPI
   - Track density ..... 135 TPI
   - Data transfer rate ..... 125K bits/sec.
4. Process time
   - Average access time ..... 710 ms
   - Track to track ..... 40 ms
   - Settling time ..... 10 ms
   - Motor start time ..... 1 sec.
5. Rotational speed ..... 300 rpm
6. Number of Indexes 2
7. Power source ..... 4 AA Alkaline batteries (Cat. No. 23-552) or AC Adapter (26-3804)
8. Power consumption
   - Operating ..... 1.8 W
   - Waiting ..... 0.08 W
   - (1) Battery life : Continuous Read/Write ..... Minimum 1.5 hours
   - : Waiting only ..... Minimum 20 hours
   - (2) Low battery : Alarm lamp average voltage ..... 4.1 V
   - : Power down average voltage 3.5V
9. Dimensions ..... 5-1/4" x 6-13/32" x 2-1/8" 133 (W) x 163 (L) x 54 (H) mm
10. Weight ..... 1 lb. 14 oz (850 grams) (Including 4 batteries)
11. Media used ..... Single-sided, 3.5-inch micro-floppy disk
12. Interface RS-232C
    - Transfer rate : Booting ..... 9600 bits/sec.
    - : Operating ..... 19200 bits/sec.

3. DISASSEMBLY INSTRUCTIONS

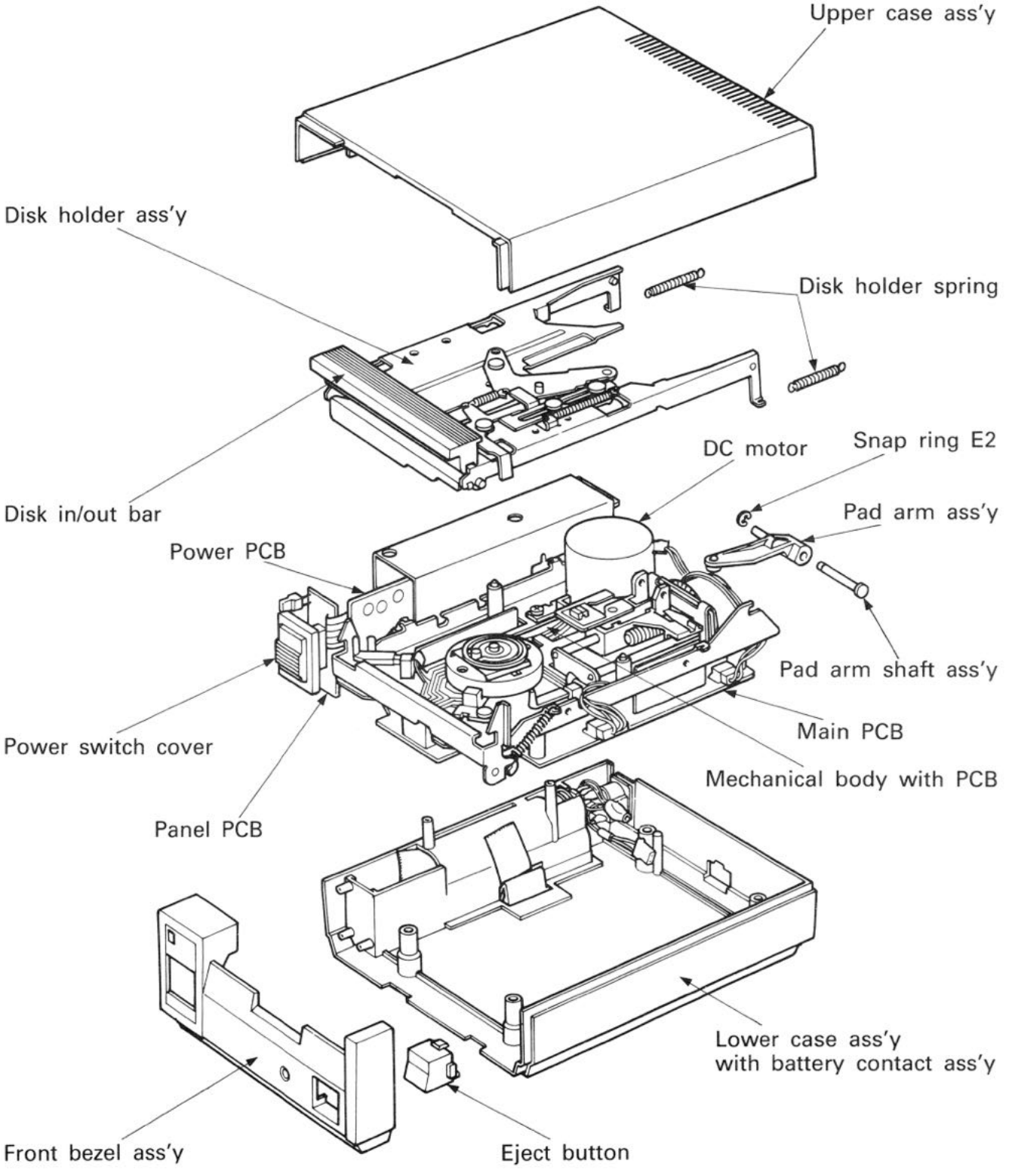


Fig. 3-1

3-1. Disassembly

Case

1. Refer to Fig. 3-2 and loosen the 2 set screws ① near the back of the lower case.
2. Remove the upper case.
3. Loosen the 2 set screws ② closest to the front edge of the lower case.
4. Remove the front bezel and the eject button.
5. Refer to Fig. 3-3 and remove the power switch cover.
6. Remove the 2 set screws ④.
7. Remove the set screw ⑤ and the collar.
8. Loosen the 2 set screws ③ near the front of the lower case. (See Fig. 3-2.)
9. Remove the connector that connects the jack and the power PCB (Fig. 3-4).
10. Detach the lower case by holding onto the mechanical body and the power circuit (Fig. 3-3), then lift up.

    Note: If the case is detached by holding onto only the mechanical body, the cable connecting the main PCB and the power PCB is likely to be damaged.

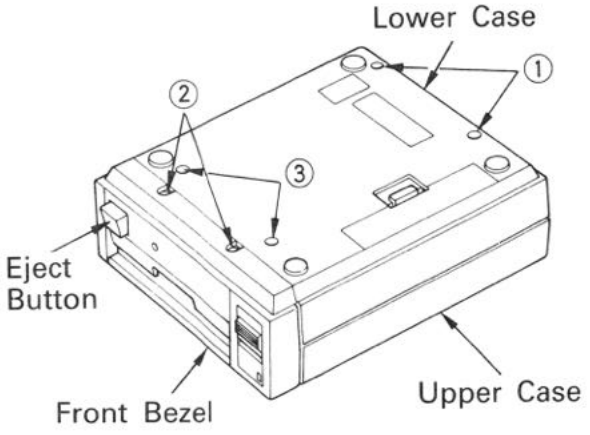


Fig. 3-2

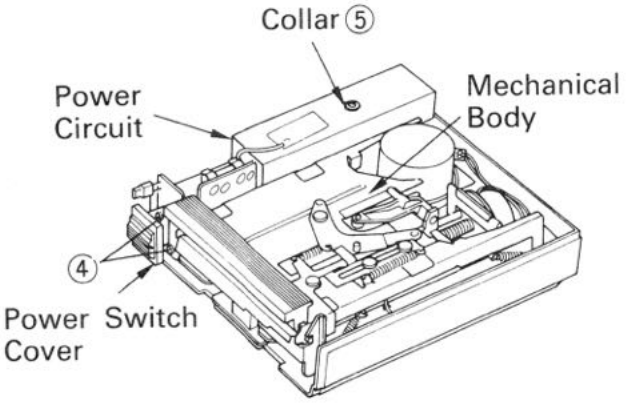


Fig. 3-3

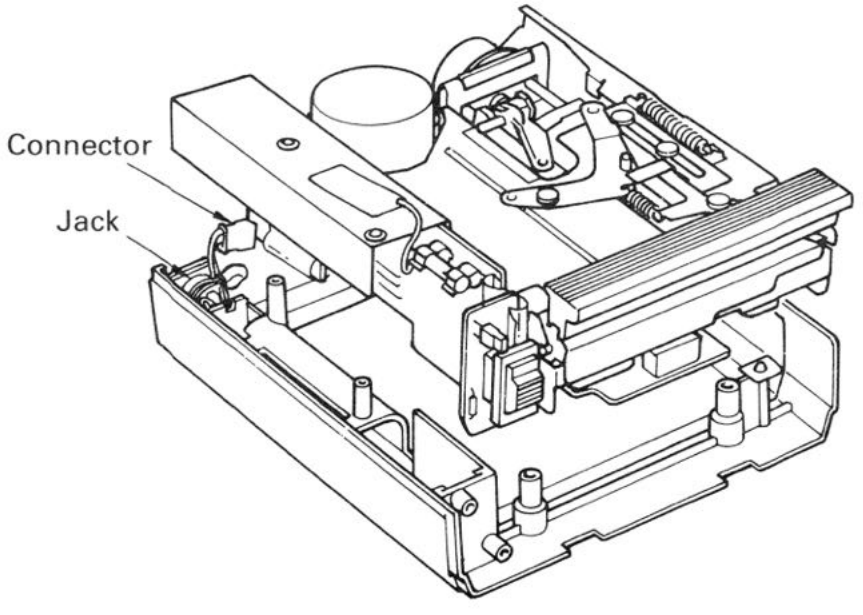


Fig. 3-4

PCB

1. Refer to Fig. 3-5 and disconnect the 3 connectors ②, ③, and ④.
2. Loosen and remove the 4 set screws ①.
3. As shown in Fig. 3-6, remove the sensor cable after pulling off the outer part of the connector ⑤ in the direction of the arrow.
4. Remove the connector which connects the main PCB and the power PCB.
5. Remove the shielded plate.
6. The jumper lead wire which connects the Panel PCB to the power PCB is soldered. Detach the wire by removing the solder.

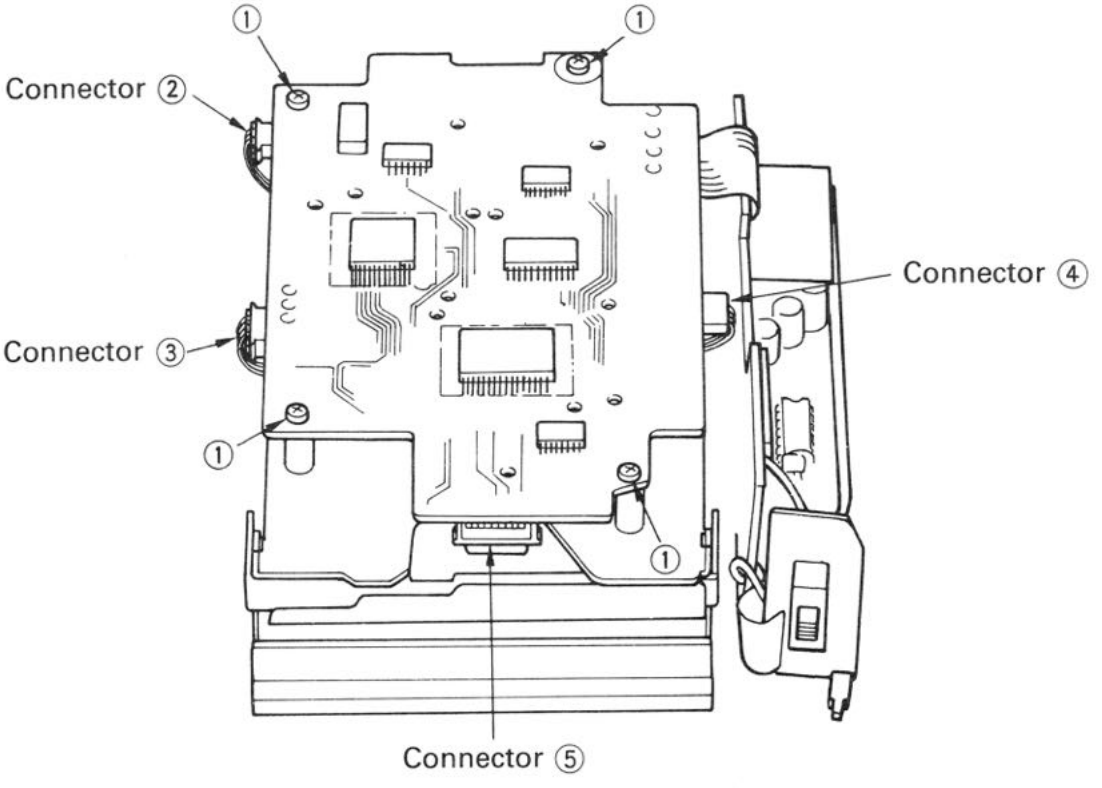


Fig. 3-5

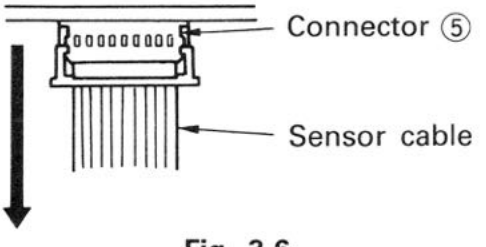


Fig. 3-6

Disk Holder

1. Remove the snap ring ① and pull out the pad arm shaft (Fig. 3-7).
2. Remove the pad arm. The pad-pressing coiled spring under the pad arm will be automatically removed with the pad arm.
3. Remove the 2 coiled springs ② and ③.
4. Remove the 2 stopper screws.
5. Release the lock of the clamping plate and remove the disk holder by pulling it backward while holding it up at about a 30-degree angle (between the chassis and the disk holder). (Fig. 3-8)

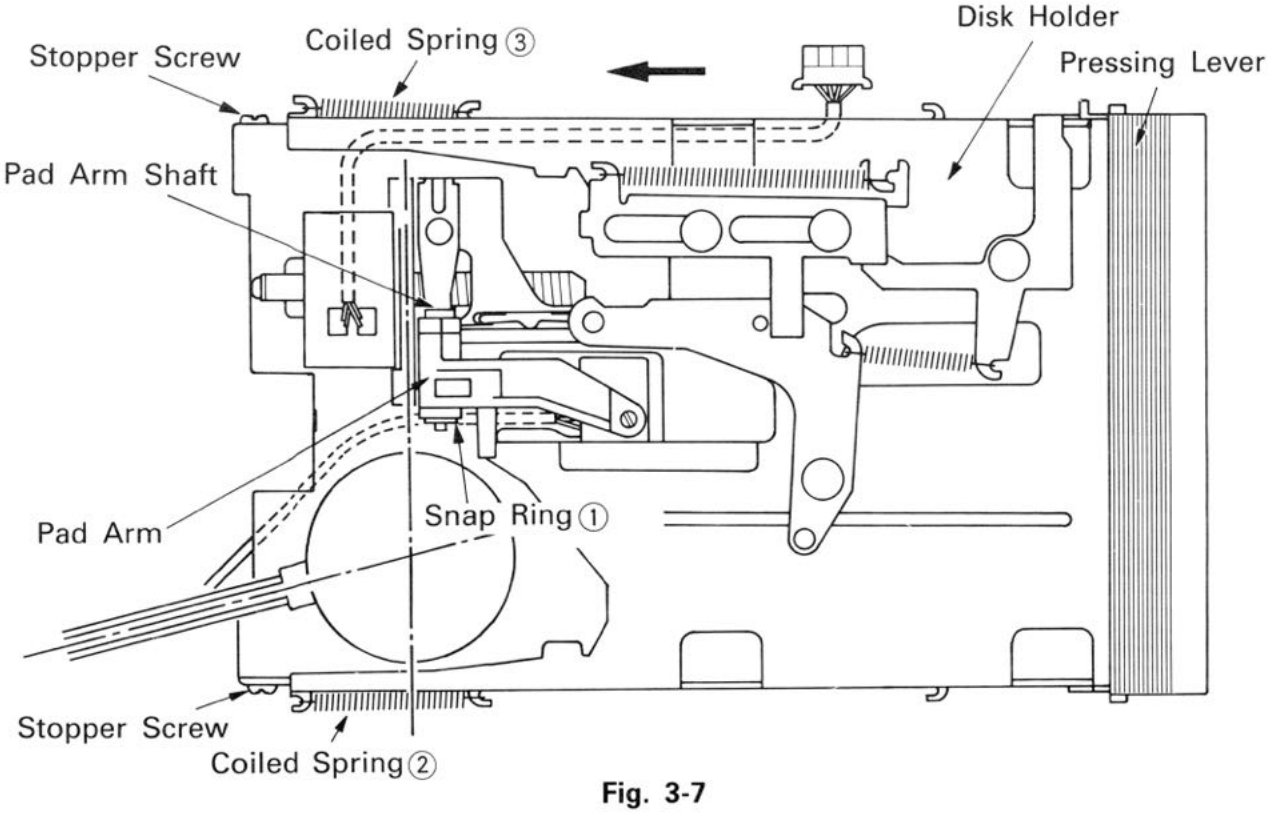


Fig. 3-7

Drive Motor

1. Remove the belt.
2. Remove the drive motor by loosening the 2 set screws.

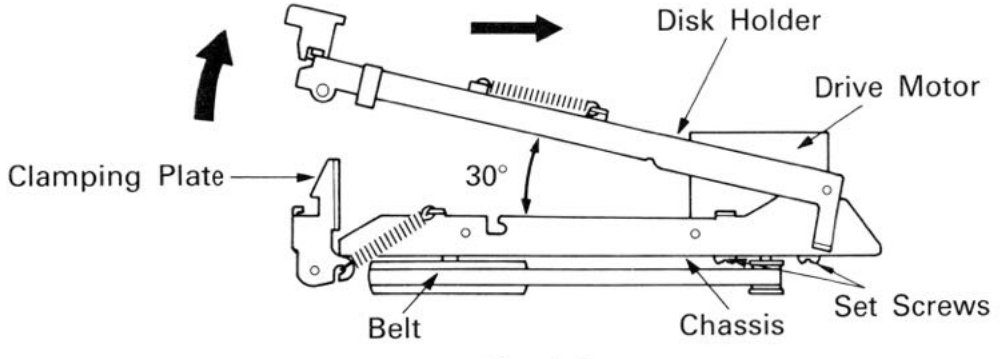


Fig. 3-8

Clamping Plate

1. Remove the 2 coiled springs on both sides of the rear portion of the unit.
2. Remove the clamping plate.

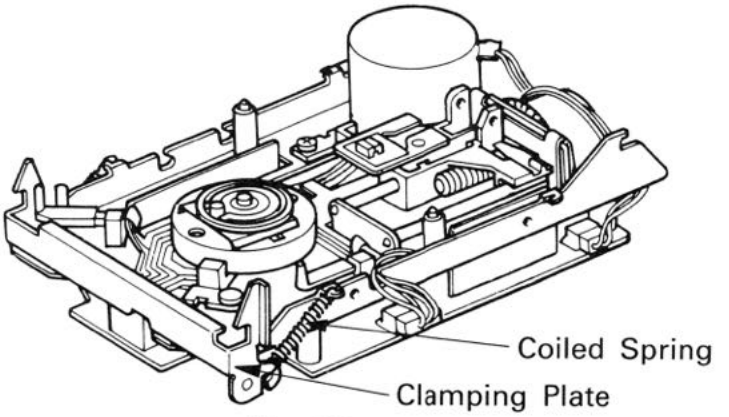


Fig. 3-9

Battery Contact

1. Remove the battery cover on the rear side of the lower case.
2. Move battery contact A in the X direction for removal (Fig. 3-10).
3. Move the jack and battery coiled spring B in the X direction for removal.
4. Remove battery contact C by moving it in the Y direction from the rear side of the lower case (Fig. 3-11).

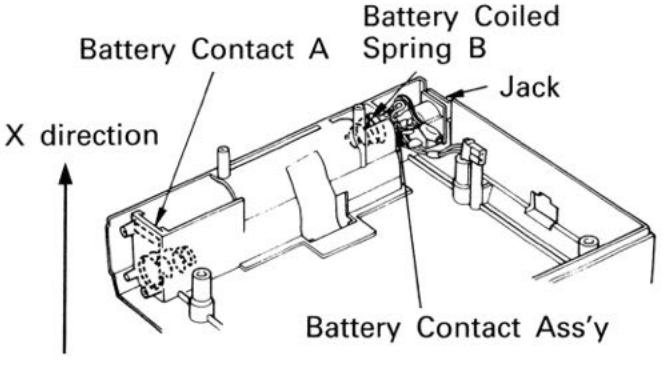


Fig. 3-10

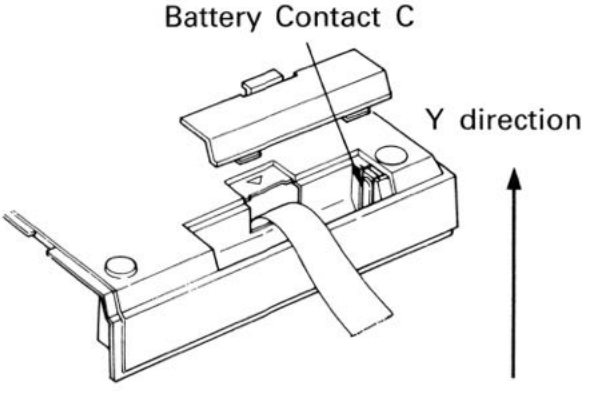


Fig. 3-11

3-2. Reassembly

Parts are reassembled in the reverse order of disassembly. The following items require additional explanation.

Drive Motor

When reassembling the drive motor, be sure that the lead wire is positioned at a 105° angle as shown in Fig. 3-12.

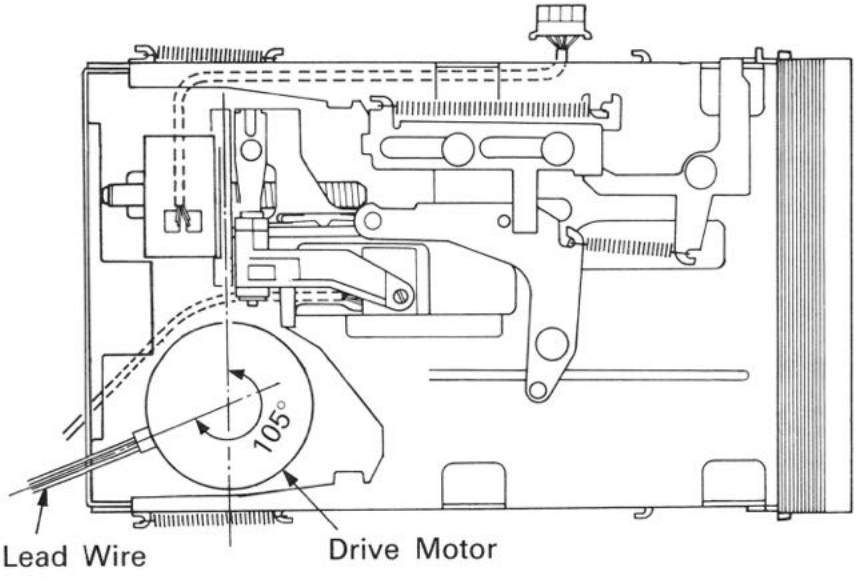


Fig. 3-12

IMPORTANT:

- Shielded Wire of the Head

  Position the shielded wire so that it will not stretch when the head is moved to the center, and so that it will not apply excessive force to the head when the head is moved to the outermost periphery (or the position of Track 0).

- Case

  Do not let the legs Ⓐ of the upper case interfere with the movement of the shielded wire of the head (Fig. 3-13). Also, be sure to provide sufficient length to the shielded wire so that it can move freely, even if the head is moved to the center.

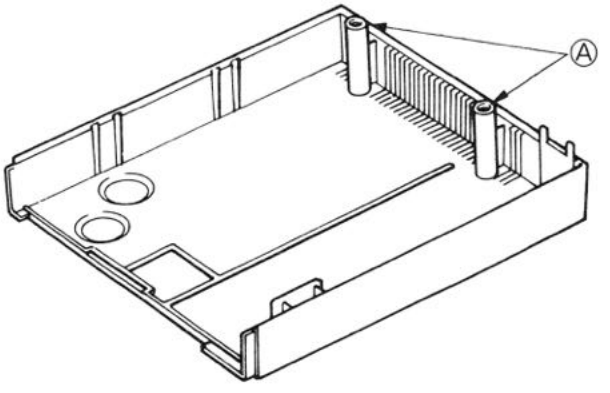


Fig. 3-13

4. BLOCK DIAGRAM

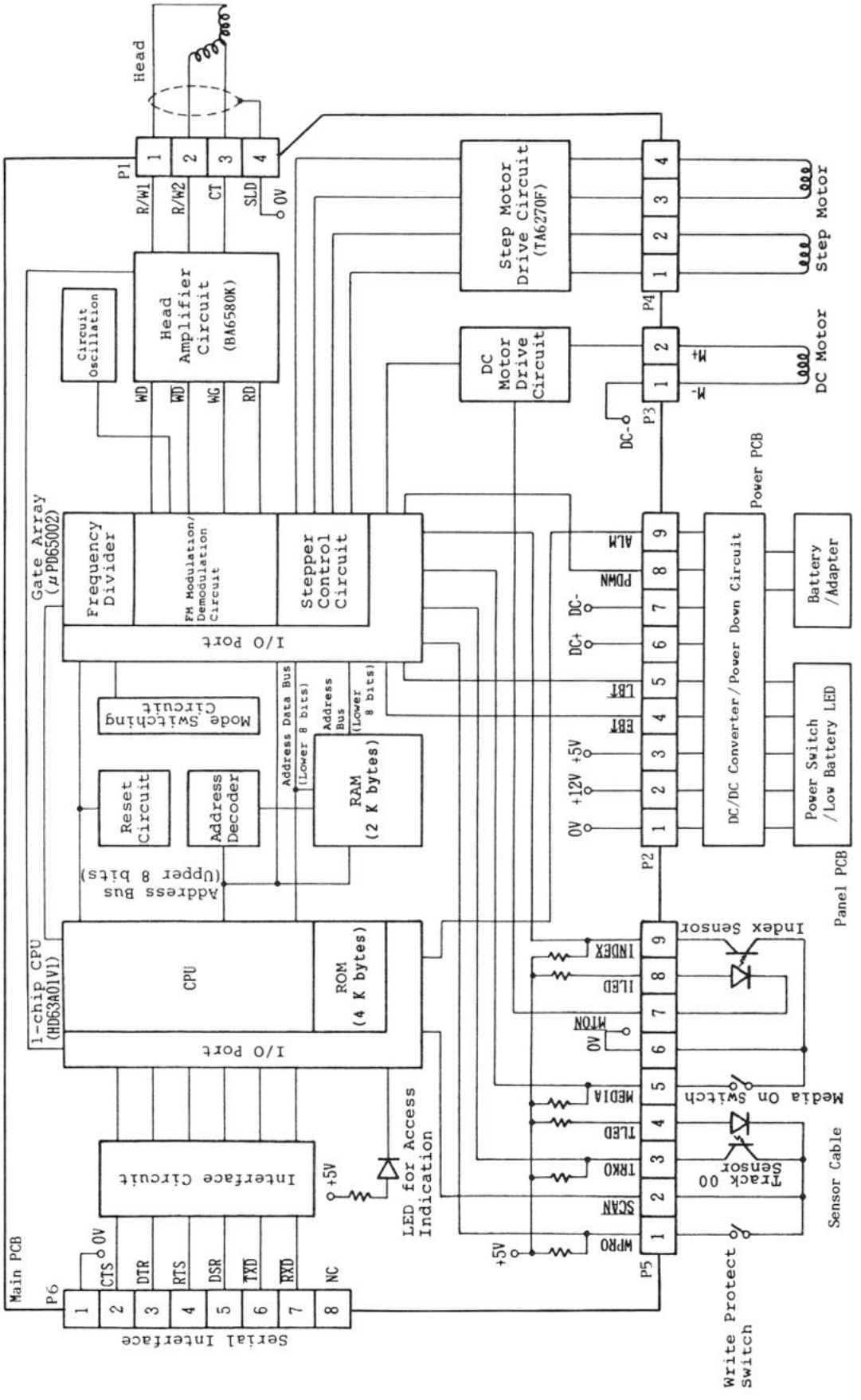


Fig. 4-1

5. PRINCIPLES OF MECHANICAL OPERATION

5-1. Structure of Disk

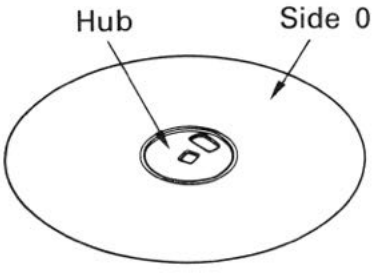


Fig. 5-1

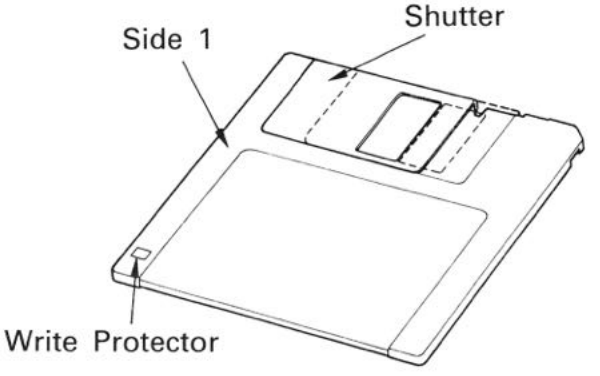


Fig. 5-2

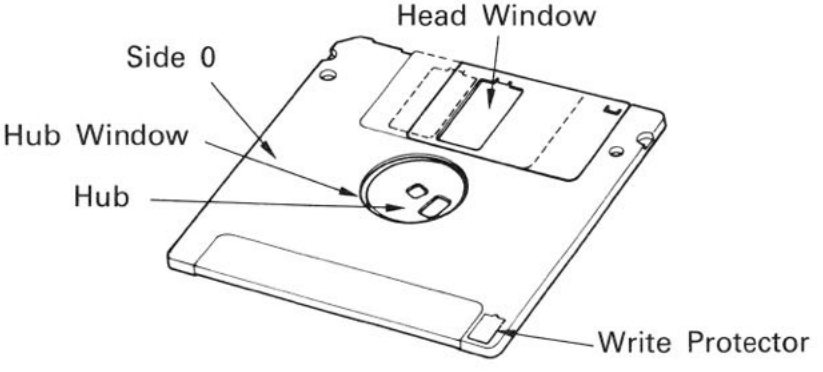


Fig. 5-3

The disk has a magnetic sheet (Fig. 5-1) protected by 2 hard plastic cases (Figs. 5-2 and 5-3). The read/write operation is performed when the shutter slides open and the head comes in contact with the disk at the head window.

5-2. Disk Driving Mechanism

The hub is made of magnetic metal and provided with 2 holes as shown in Fig. 5-3. The spindle shaft goes into the center hole and the drive pin into the adjacent hole (Fig. 5-4). When the disk is inserted into the disk drive, the hub is attracted by the magnetic chuck. The spindle rotates clockwise and the drive pin moves into the positions shown in Figs. 5-5 and 5-6. When the disk is correctly centered, the spindle shaft touches the edge of the square hole at points a and b (Fig. 5-6) and the drive pin touches the edge of the longer hole at points c and d. Thus, unwanted side-to-side motion is prevented, even though the spindle rotates at 300 rpm.

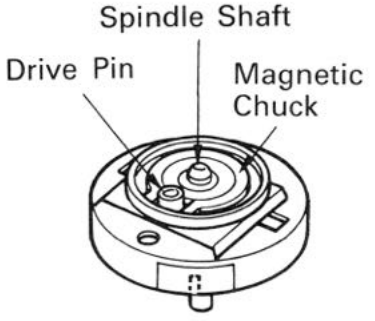


Fig. 5-4

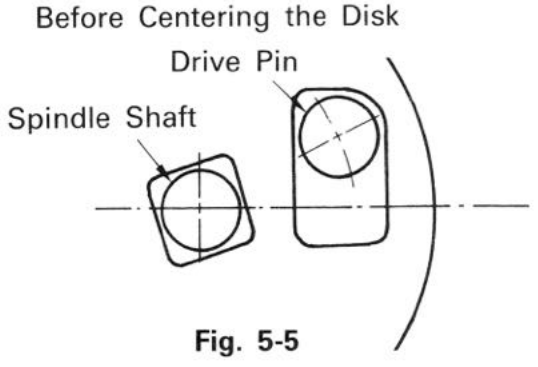


Fig. 5-5

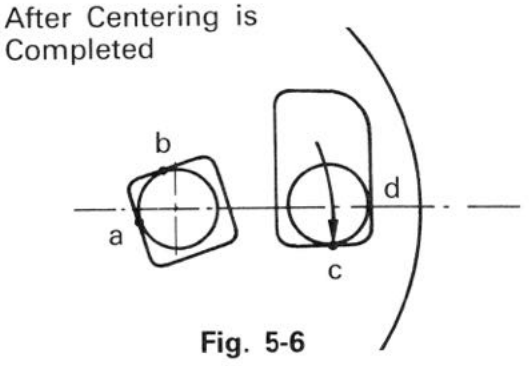


Fig. 5-6

5-3. Head Positioning Mechanism

The head attached to the carriage is positioned by the stepping motor and the lead screw. When the stepping motor is supplied with 1 pulse, the lead screw rotates 15° and the head moves 0.046875 mm with the aid of a steel ball. The head moves 1 track (0.1875 mm) when the stepping motor receives 4 pulses. The Portable Disk Drive 2 is designed so that the head always moves outward for more accurate positioning. To move the head from Tr0 to Tr1, 6 pulses are actually required. The head advances from Tr0 by 5 pulses, thereby moving beyond Tr1 by 1 pulse, and then it returns to Tr1 by 1 additional pulse for more accurate positioning.

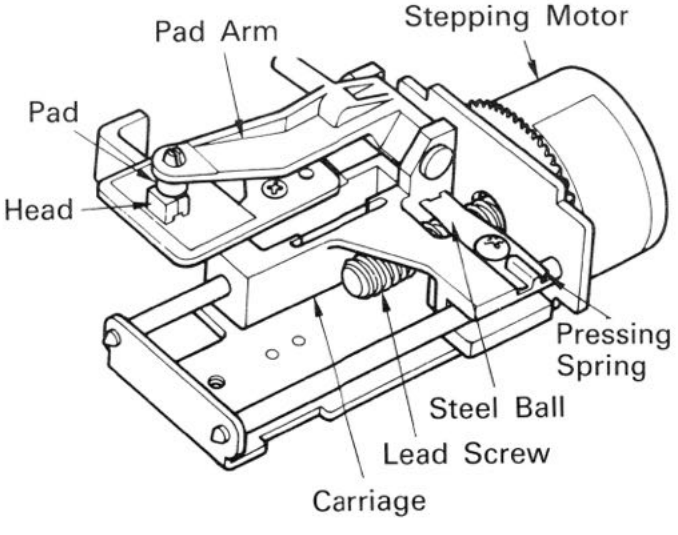


Fig. 5-7

5-4. Structure of Read/Write Head

The read/write head is always in contact with the disk by means of a head pad. The surface of the head is designed so that the wear of the head and the disk are at a minimum and that the signal for reading data from the disk is at a maximum.
The Portable Disk Drive 2 has a single gap head without an erase gap; the read, write and erase operations are all performed by 1 coil (Fig. 5-8). The head moves 1 pulse inward (0.046875mm) and 2 pulses outward to erase; then it moves 1 pulse inward to write the data (Fig. 5-9). Therefore, it is possible to read the data even if tracking is off, because the data area is located between the erased areas.

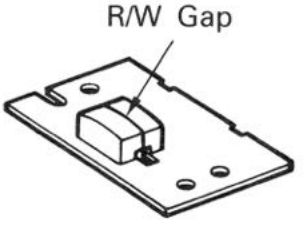


Fig. 5-8

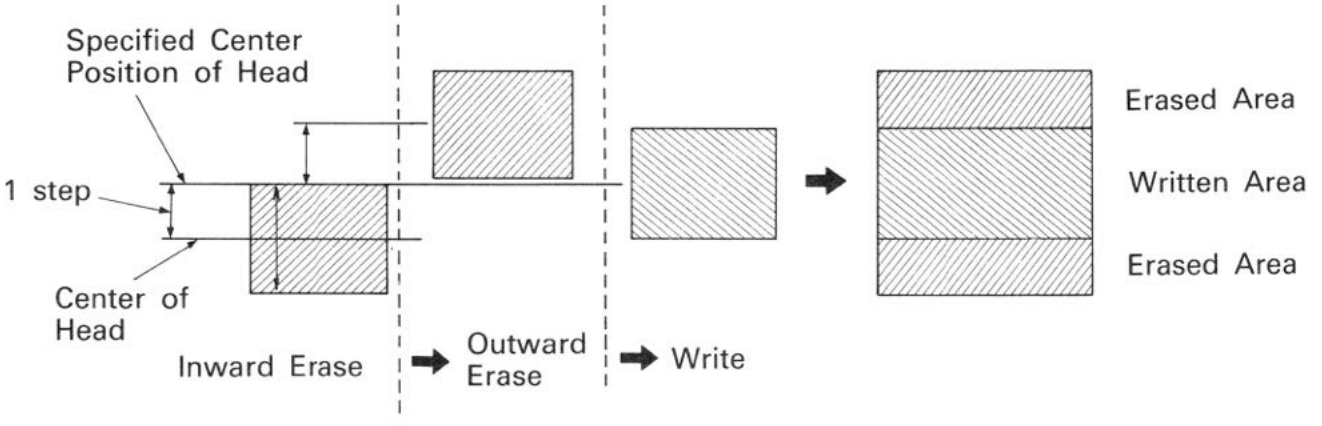


Fig. 5-9

5-5. Pad Mechanism

The read/write head comes into contact with the disk while the head pad pushes the disk from the upper side. The material and shape of the pad, and the strength of the pad arm spring, are designed so that the head receives the most adequate signal from the disk during the read/write operation.

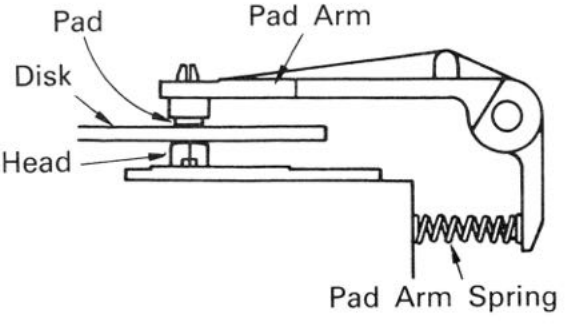


Fig. 5-10

5-6. Disk Eject Mechanism

When the disk is entirely inserted into the holder, the loading click and loading plate are engaged and locked. When the disk in/out lever is pushed downward, the clamp plate and cylindrical convex part of the disk holder are engaged and locked.

When the eject button is pressed, the clamp plate is released from the cylindrical convex part of the disk holder and the loading click is released from the loading plate.
Then the disk holder is raised by the coiled spring ① and the disk is pushed out by the loading plate connected to another coiled spring ②.
This is how the disk is ejected.

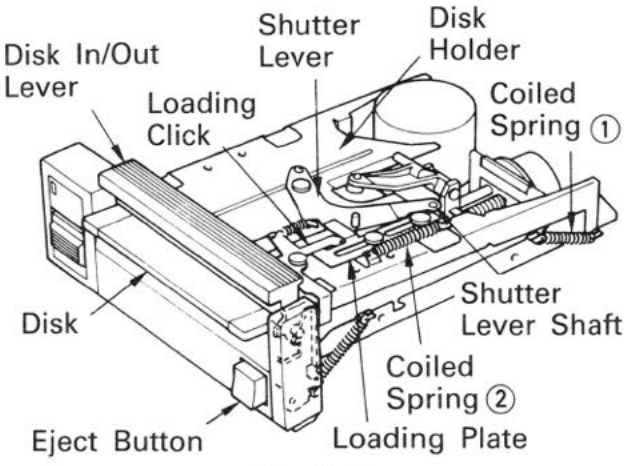


Fig. 5-11

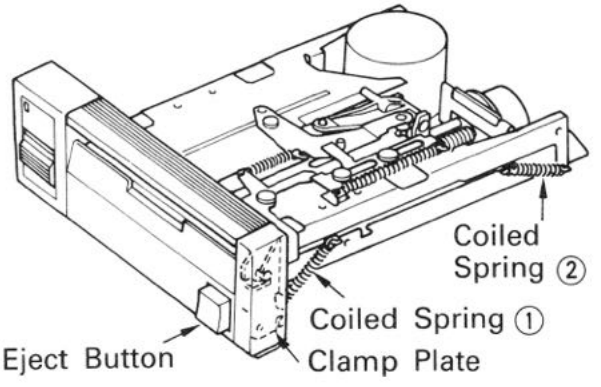


Fig. 5-12

5-7. Write Protector

The disk is provided with the sliding-type write protector (Fig. 5-13).
When this shutter slides open, the disk is in a state of write protection. The Portable Disk Drive 2 detects this window with the write-protect detection switch.

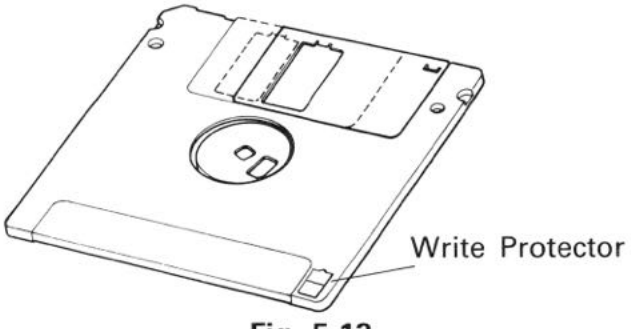


Fig. 5-13

5-8. Index

The disk drive requires an index signal for read/write operations.
To detect the index signal, an index sensor searches for a big notch and a small one provided on the side face of the encoder (Fig. 5-14).

5-9. Disk Detection

When the disk is inserted and locked into regular position, the disk detection switch is pressed by the disk.
This switch detects whether or not a disk is in the disk drive.

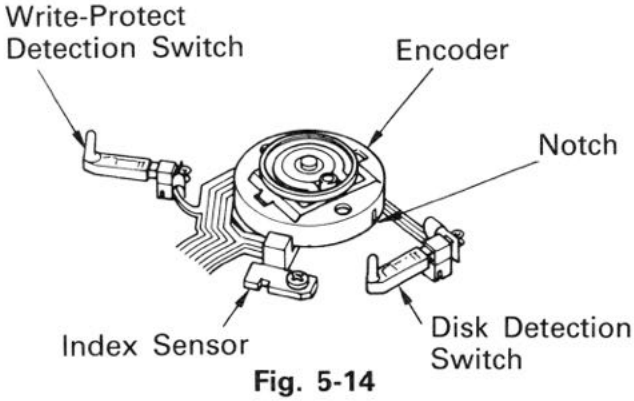


Fig. 5-14

5-10. Home Position Return

When the disk drive is supplied with power, the carriage returns to Tr0 (track 0).
When the carriage moves to the right and the covering part (a) in Fig. 5-15 covers the slit of the Tr0 sensor, the read/write head is positioned at Tr0.

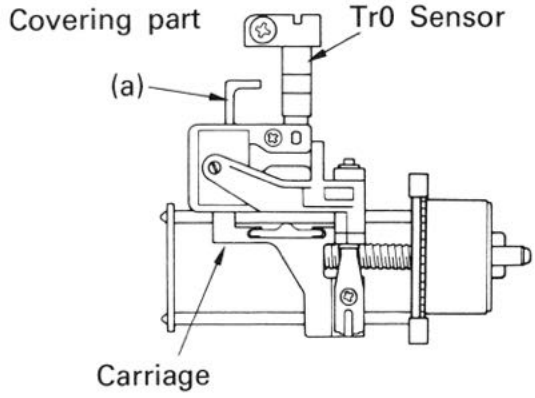


Fig. 5-15

6. PRINCIPLES OF ELECTRONIC OPERATION

6-1. Electronic Components

The electronic section consists of 3 PCBs (printed circuit boards) (See Fig. 6-1.):

- Main PCB
- Panel PCB
- Power PCB

The Panel PCB has a flat cable which connects with the Power PCB.

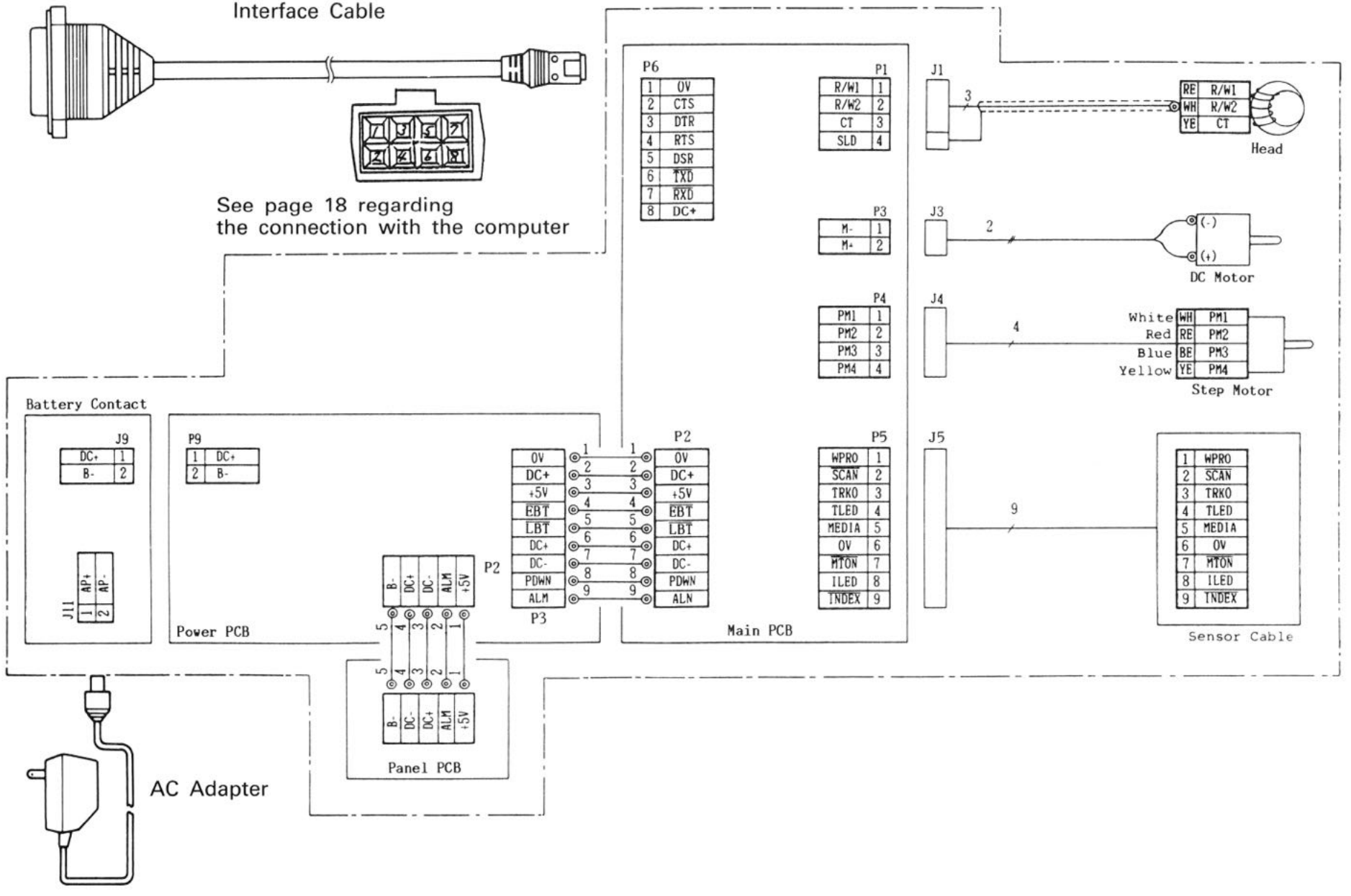


Fig. 6-1 Connection Diagram

6-2. Main PCB

The main PCB controls the entire system and consists of an interface circuit, 1-chip CPU, gate array, read/write amplifier, step motor driver, RAM, oscillation circuit, reset circuit and address decoder.

6-2-1. Interface Circuit

Fig. 6-2. is an input and output circuit which shows the connection with a host (for example, a Model 100) by a pseudo RS-232C interface. (See the schematic diagram of the main PCB in Fig. 12-1 on page 67.)

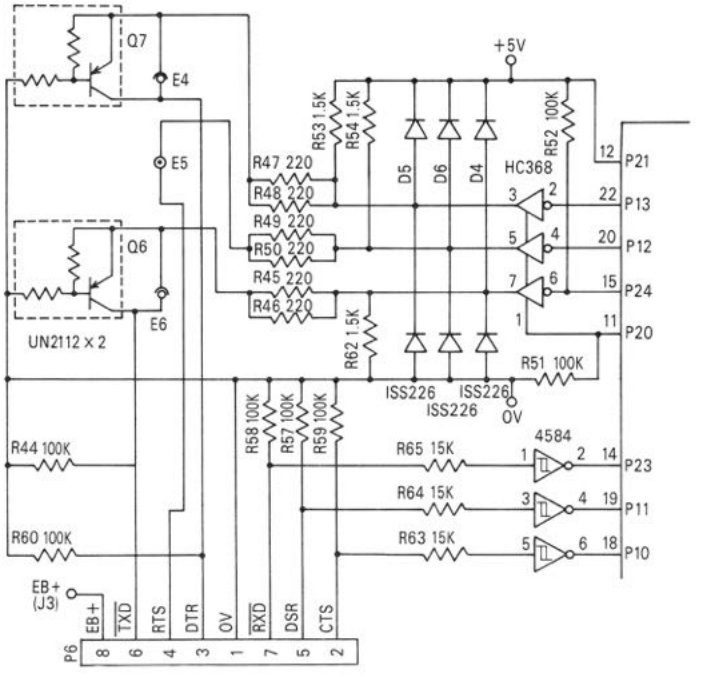


Fig. 6-2

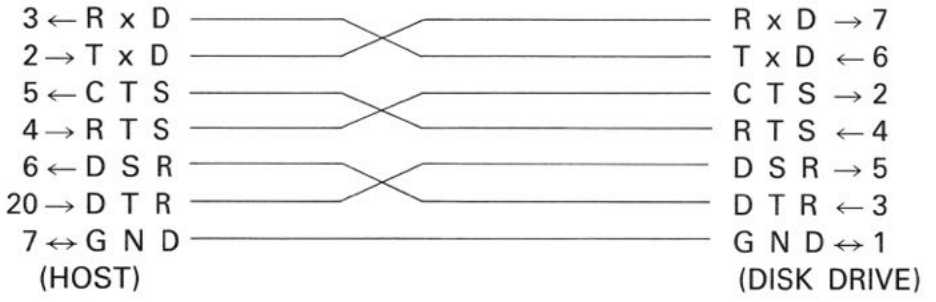
R45 to R50 are protective resistors for output short.
D4 to D6 are diodes to protect the IC (HC368) from latch-up.
R63 to R65 are protective resistors; the input voltage can be used with a variation of up to ±12V.
Q6 and Q7 are signal level converters for the Model 100 and/or Tandy 200 interface circuit.
R53 and R54 are pull-up resistors.
R57 to R59 and R62 are pull-down resistors.

Electrical Characteristics

Output	$V_{OH} \approx 4.5V$ ($I_{OH} = -2.5mA$)	$V_{OH} \approx 5 + 0.2I_{OH}$
	$V_{OL} \approx 0.5V$ ($I_{OL} = 3mA$)	$V_{OL} \approx 0.16I_{OL}$
Input	$6V < V_{IH} < 12V$	$I_{IH} \approx (V_{IH} - 5.7)/15K$ (mA)
	$-12V < I_{IL} < 1V$	$I_{IL} \approx (-0.7 - V_{IL})/15K$ (mA)
		(where $-12 < V_{IL} < -0.7$)
		I_{IL} 100μA
		(where $-0.7 < V_{IL} < 1$)

The sequence of the signal conforms to RS-232C.

Connection with Host



Communication Method

Half-Duplex, Start-Stop Synchronization (See pages 39~41 for details.)

1 Start Bit, 8-Bit Data, 1 Stop Bit without Parity

Transfer Rate

Operating 1200, 4800, 9600, 19200 bps

6-2-2. One-Chip CPU (HD6301V1)

This 8-bit central processing unit (CPU) controlling the system of the disk drive has one serial interface, several I/O ports, 4K bytes of mask programmed ROM, and 128K bytes of RAM. The functions of each terminal will be described later. This CPU functions at mode 6. The 8 bits of data and the lower 8 bits of address lines are multiplexed. Fig. 6-3 shows the bus timing. The lower byte of the address is determined at the falling edge of AS. The read/write operations of the data are performed at the falling edge of E. This IC is made by the CMOS process, so that it consumes less power.

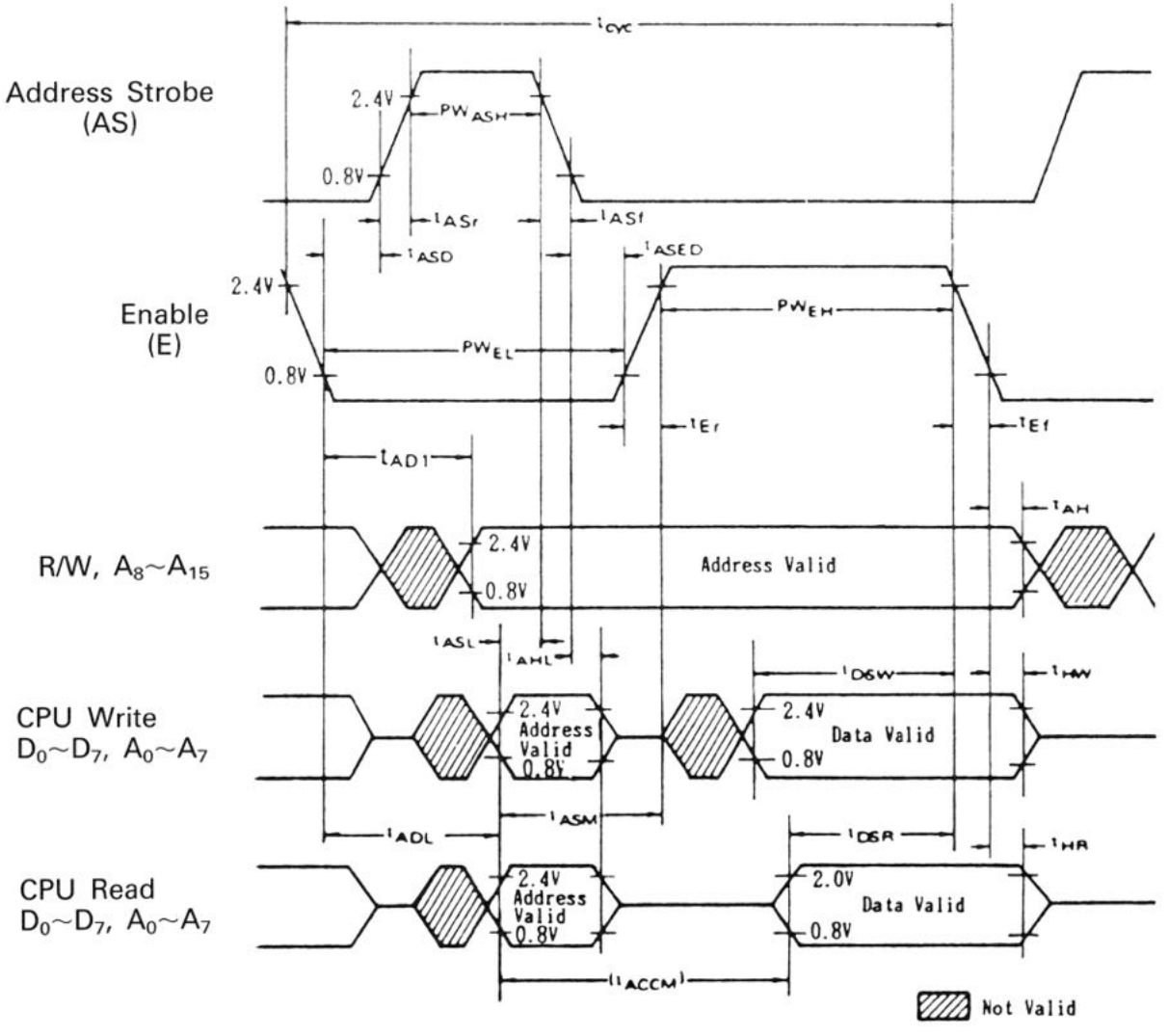
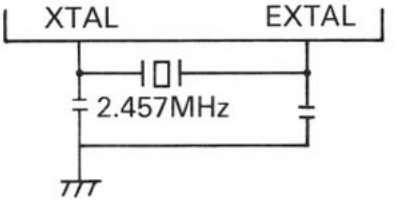
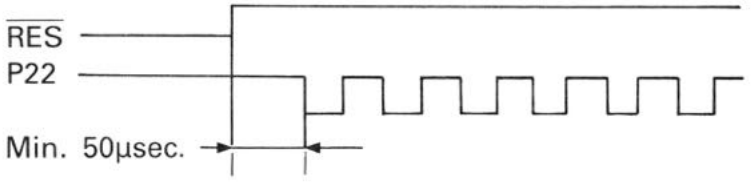


Fig. 6-3

Terminal and Function CPU (HD6301V1)

Terminal	Pin No.	Function
$\overline{NMI}$	4	Non-maskable interrupt input. This unit does not use this terminal. Always high level.
$\overline{IRQ}$	5	Interrupt input. This unit does not use this terminal. Always high level.
GND	1	Ground
XTAL	2	Clock input for CPU. Oscillation is generated by the ceramic resonator of 2.457MHz.
EXTAL	3	Clock input for CPU. This is also used with the oscillator. 
$\overline{RES}$	8	Reset input. The low level is held for 20msec. or more after the unit is powered on, then changes to the high level.
$\overline{STBY}$	9	Stand-by input terminal. This terminal is not used. Always high level.
P20	11	When resetting, this port works as a mode setting input port. During this time its level is set to low. When the CPU is operating, this port works for serial interface control.
P21	12	Input port to set the mode of the CPU. Always high level.
P22	13	When resetting, this input port sets the mode of CPU. After resetting, it is the input port for the standard clock of the serial interface (8 times the baud rate). Duty of the standard clock: 50%. The timing is as follows: 

Terminal	Pin No.	Function
P23 (RxD)	14	Input port to receive the data of the serial interface. High level when there is no communication with the host.
P24 (TxD)	15	Output port to transmit the data of the serial interface. High level when there is no communication with the host.
P10 (CTS)	18	Input port to receive the request to send signal which is the interface control signal from the host.
P11 (DSR)	19	Input port to receive the data terminal ready signal from the host.
P12	20	Output port to permit the transmission to the host.
P13 (DTR)	22	Output port to indicate this unit is powered. Always high level after the power is supplied.
P14 (ALM)	23	When the LBT (low battery) signal from the power PCB is high level, the CPU recognizes the low battery state and sets this terminal to high level to light the low battery LED. The CPU detects the LBT signal only while the serial interface is awaiting input or during input. This signal is not detected during the seeking, reading or writing operations.
P15 (WC)	24	Output port to control head write current. When the read/write head is located from track 0 to track 59, its level is low; and when it is located from track 60 to track 79, its level is high.
P16	25	The output is low level when reading or writing from/to the disk. The CPU shuts down the reading or writing circuit to save power while the output is high level. This port also controls access indicator LED and clock oscillator for modulation and demodulation.
P17 (SCAN)	26	The output is high only when detecting the track 0 (zero) signal and the write-protect signal. During low levels, the track 0 sensor and the write-protect switch are not supplied with electricity to save power.
Vcc	27	+5V of the power supply.
	6,7,10,16, 17,21,33, 34,38,39, 46~49	These pins are non-connected.

Terminal	Pin No.	Function
A15	28	A14, A15 of the address bus.
A14	29	
A13	30	Mode setting input ports for CPU operation.
A12	31	
A11	32	
A10	35	A10, A9, A8 of the address bus.
A9	36	
A8	37	
AD7	40	The lower 8 address bits and the 8 data bits are multiplexed.
AD6	41	
AD5	42	
AD4	43	
AD3	44	
AD2	45	
AD1	50	
AD0	51	
R/$\overline{W}$	52	The read/write signal of the CPU. The low level is output in writing and the high level in reading. The high level is also output during reset.
$\overline{AS}$	53	Strobe signal output to separate the address bus from the address/data bus.
E	54	Output of system clock. The frequency of 2.45MHz is divided by one fourth. The RAM and the gate array are accessed when this clock is high. The data is read/written from/to them at the falling edge of this clock.

6-2-3. Gate Array (μPD65002G)

The gate array of 857 gates is made through the CMOS process. It consists of the input port, the output port, the dividing circuit, the FM/MFM modulation/demodulation circuit, and the address (lower 8 bits)/data separating circuit. Refer to the following table for the functions of each terminal of the gate array.

Gate Array (μPD65002) Terminals and Functions

Terminal	Pin No.	Function
RD	1	Modulated signal input which is read out of the disk. Pulse width: 250μsec. Pulse interval: approx. 4μsec. or 8μsec.
$\overline{WE}$	2	Low level output when writing to the disk. The writing circuit functions when $\overline{WE}$ = low.
WD	3	Modulated data output for writing to the disk. The $\overline{WD}$ is an inverted signal of the WD and vice versa. The width of the high and low levels is 4μsec. or 8μsec. during writing. And the level is fixed at high or low during erasing.
$\overline{WD}$	4	
AD0	8	Address (lower 8 bits)/data bus. Used to input or output the multiplexed signals.
AD1	6	
AD2	5	
AD3	52	
AD4	51	
AD5	50	
AD6	49	
AD7	48	
Vcc1	33	+5V power supply.
Vcc2	7	
A7	9	Address bus (lower 8 bits). The AD0–AD7 are latched by the AS as address signal. A0 and A1 are used as signals to select the internal register.
A6	10	
A5	11	
A4	12	
A3	13	
A2	15	
A1	16	
A0	17	
$\overline{TRK0}$	18	To input the low level when the head is at track 0. Therefore, this signal changes from high to low while the head moves from track 1 to 0. This signal is valid, however, only when the SCAN signal is active (CPU P17 is high level) because the sensor circuit is not supplied with power when SCAN = Low.

Terminal	Pin No.	Function
MTON	19	The DC motor rotates when a high level signal is output. The index signal is valid only when this signal is high. The index sensor stops to save power during low levels.
ϕ	20	Standard clock input of 8 MHz.
COMP0	21	The low level is input when the battery voltage drops to 3.5V or less. When this signal is input, the PWD outputs the high level to turn off the power.
COMP1	22	The low level is input when the battery voltage drops to 4.1V or less. When this signal is input, battery replacement is required. P15 of the CPU changes to the low level to indicate low battery status.
PD	23	Usually low level after power is supplied. If the power voltage is insufficient, the low level signal is input from COMP0 and PWD outputs the high level to turn off power.
RES	24	The reset signal input. A low level input makes all functions return to their states: CL OUT = high, PWD = low, $\overline{WE}$ = high, and $\overline{STEP0}$ – $\overline{STEP3}$ = high, RES goes high level 20msec. or more after the power is supplied.
SCLK0	25	SCLK0, SCLK1, SCLK2 and SCLK3 are input ports that determine drive interface mode. In connecting Portable Disk Drive 2 with Model 100/102, Tandy 200, these pins are pulled up to +5V.
SCLK1	26	
SCLK2	27	
SCLK3	28	

Terminal	Pin No.	Function
WPRO	29	Write-protect signal input. A high level signal creates a write-protect state. Valid only when the SCAN is high since the switch is not supplied with power when SCAN is low.
TESTM0	30	Input terminal to check the gate array by manufacturer. Direct connection with the ground.
TEST0	31	
WINDOW	32	Window signal input terminal for MFM demodulation. Direct connection with the ground because of FM modulation.
GND	34	Ground
$\overline{\text{STEP0}}$	35	Output for the excitation of the step motor. Phase excitation is possible when $\overline{\text{STP0}}$ and $\overline{\text{STP2}}$ are in an inverted relationship with $\overline{\text{STP1}}$ and $\overline{\text{STP3}}$, respectively. Refer to the software manual for details on the output stage.
$\overline{\text{STEP1}}$	36	
$\overline{\text{STEP2}}$	37	
$\overline{\text{STEP3}}$	38	
$\overline{\text{MDIN}}$	39	Signal input detects whether the disk is set in the unit. A low level indicates the loading of the disk. The unloading of the disk (the rise of the signal) is detected by the D-FF. The change of the disk is also detected. Detection is performed by the mechanical switch.
INDX	40	Index signal input. Two types of pulses, a long one and a short one, input per one rotation of disk. Pulse length: approx. 6msec. and 3msec.
$\overline{\text{CS0}}$	42	Signal input to select the register of the gate array. $\overline{\text{CS0}}$ is the low level and CS1 is high for selection of the register.
CS1	41	
CLKIN	44	Standard clock input for the CLKOUT. The signal from CLKIN is divided by 2^n (where n is software selectable) and provided for CLKOUT.
CLKOUT	43	Standard clock output for the serial interface. The mode of the CPU is set at the high level during reset.
E	45	System clock input from the CPU. When this signal is high, the register is accessed.
$\overline{\text{AS}}$	46	Control signal input to separate the address (lower 8 bits) and the data bus.
R/$\overline{\text{W}}$	47	Signal input to read and write in the register. High level in resetting.

6-2-4. Step Motor Drive Circuit

The step motor drive circuit is constituted as shown in Fig. 6-6.
R7, Q1 and Q2 cause the drive voltage of the step motor to drop from 5V to about 3.6V. TA6270F is a transistor array and its internal connection is shown in Fig. 6-7.
D1 and D2 absorb the spike which occurs when the excitation phase is changed.

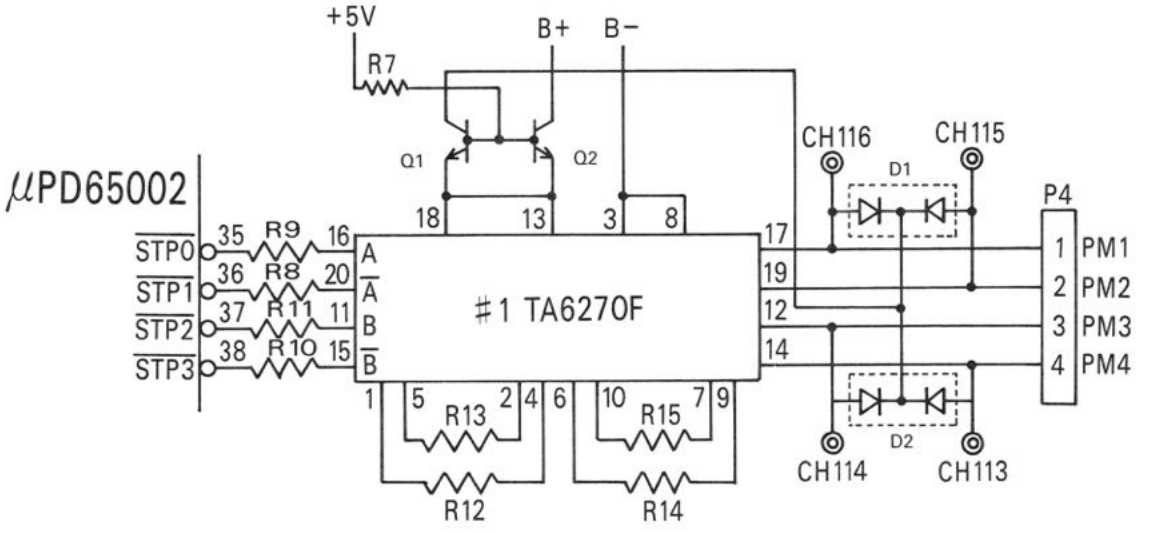


Fig. 6-6

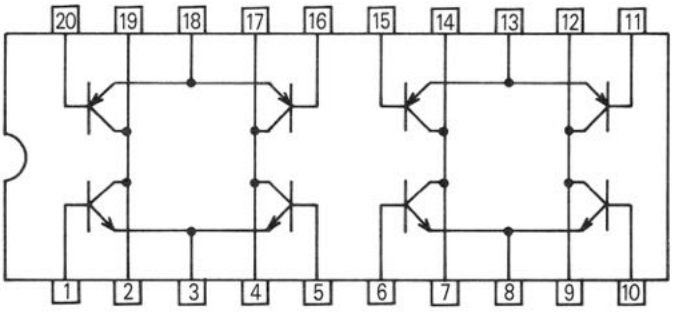


Fig. 6-7

6-2-5. Read/Write Amplifier Circuit IC (BA6580K)

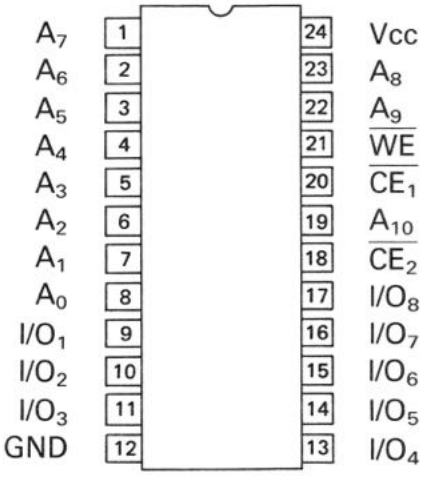
Signal	Pin No.	Function
RW01 RW02	12 13	SIDE0 Read/Write Head connection terminal.
COM0	21	SIDE0 Read/Write Head common connection terminal.
RW11 RW12	14 15	SIDE1 Read/Write Head connection terminal. (Portable Disk Drive 2 does not use it.)
COM1	19	SIDE1 Read/Write Head common connection terminal. (Portable Disk Drive 2 does not use it.)
GS0 GS1 GS2	9 8 7	Read pre-amplifier gain selection terminal. GS0–GS1 connection set a gain of 100. GS0–GS2 connection set a gain of 200. Portable Disk Drive 2 connects 7–9 and uses a gain of 200.
PRE OUT1 PRE OUT2	6 5	Read pre-amplifier. Differential output terminal.
DIFF IN1 DIFF IN2	3 4	Derivative differential input terminal.
DIFF CONST1 DIFF CONST2	2 1	Derivative constant connection terminal.
DIFF OUT1 DIFF OUT2	44 43	Derivative differential output terminal.
COMP IN1 COMP IN2	41 42	Comparator differential input terminal.
TDF COMP	40	Connects the resistor to revise a time constant of the time domain filter circuit.
TDF CR	39	Connects a C-R time constant for the time domain filter.
RDO CR	37	This terminal is connected with the C-R time constant for read-data pulse width.
READ DATA	33	Read-data output signal. This signal level is TTL-compatible.
$\overline{\text{TDF CONT}}$	35	This input signal controls the time constant of the time domain filter. When this input signal is low, the time constant will be reduced.
$\overline{\text{OC}}$	34	This input signal controls the read-data output (33) feature. When this input signal is low, read-data output is active.

Signal	Pin No.	Function
WC SET	26	This terminal is connected with the resistor that determines the write current of the R/W head.
WC COMP	25	This terminal is connected with the resistor that revises the write current of the R/W head.
$\overline{\text{WC CONT}}$	27	This input signal controls the write current of the R/W head.
$\overline{\text{WC GATE}}$	29	When this terminal is low level, BA6580K operates as a write amplifier.
$\overline{\text{W DATA}}$	28	This terminal receives the write data signal.
WR DUMP	17 18	These terminals are connected with the write dumping resistor.
$\overline{\text{E GATE}}$	30	When this terminal is low level, the erase gate will open. (Not used.)
EO 0	24	Erase current sink terminal for SIDE0 of the R/W head. (Not used.)
EO 1	25	Erase current sink terminal for SIDE1 of the R/W head. (Not used.)
VCC1	36	+5 volt supply for the digital circuit.
VCC2	20	+5 volt supply for the write circuit.
VCC3	10	+5 volt supply for the analog circuit.
ANA GND	16	Analog ground.
DIG GND	38	Digital ground.
ERA GND	23	Erase ground.
$\overline{\text{SIDE1}}$	31	When this terminal is low level, the R/W head of SIDE1 is selected. In this circuit, this terminal is connected to VCC and always selects the R/W head of SIDE0.
$\overline{\text{POWER DOWN}}$	32	When VCC1 and/or VCC2 is less than about 3.9V, this output goes low level. (Not used.)

6-2-6. RAM (HM6117FP4)

All circuits of the static RAM are made through the CMOS process to achieve a power-saving operation.

Connection Diagram (Top View)



$A_0 - A_{10}$: Address input
$I/O_1 - I/O_8$: Data input and output
CE_1, CE_2 : Chip enable input 1 and 2
WE : Write enable input
Vcc : Power source of +5V
GND : Ground

Fig. 6-9

6-2-7. Oscillation Circuit

This circuit is constituted as shown in Fig. 6-10.
It generates an 8 MHz square wave by the ceramic oscillator which includes a capacitor. P16 of the CPU can stop oscillation.
When P16 is in high level, the circuit oscillates.
When P16 is in low level, the circuit stops oscillation.

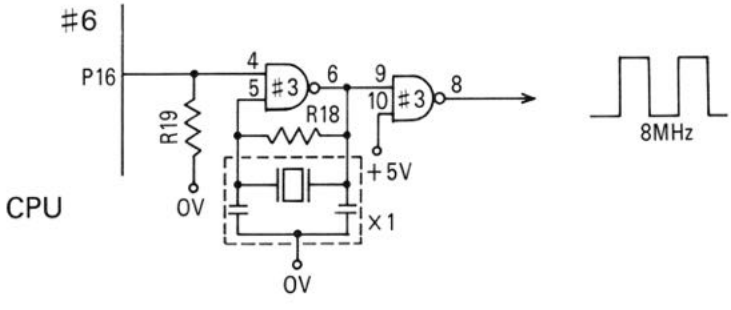


Fig. 6-10

6-2-8. Reset Circuit (M51953AFP)

Through the delay capacitor, which is connected to pin 5, the reset signal (active low) occurs for about 75ms when power is turned on.

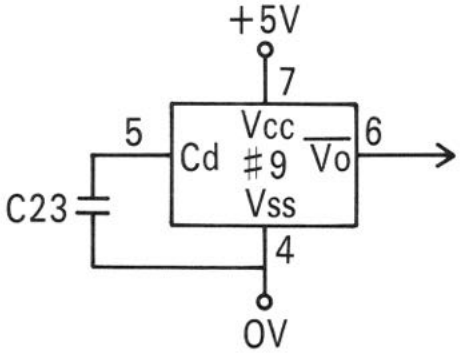


Fig. 6-11

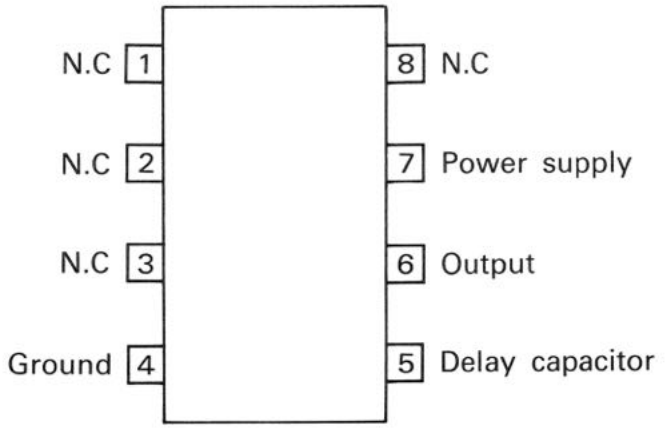


Fig. 6-12

Operation of reset circuit

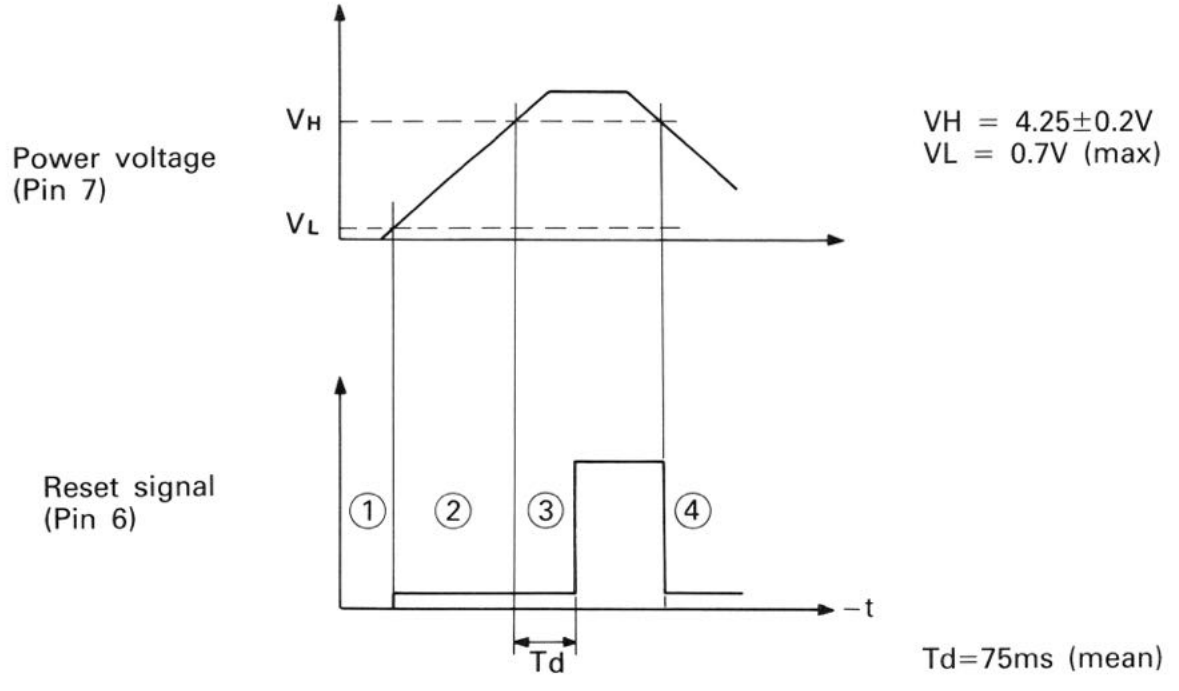


Fig. 6-13

① When power voltage is lower than V_L, the reset signal is unknown.
② When power voltage is lower than V_H, the reset signal is low level.
③ After power voltage reaches V_H, the reset signal remains low level for Td, then change to high level.
4 If power voltage goes lower than V_H, the reset signal changes to low level immediately.

6-2-9. Address Decoder

Fig. 6-14 shows the address decoder.

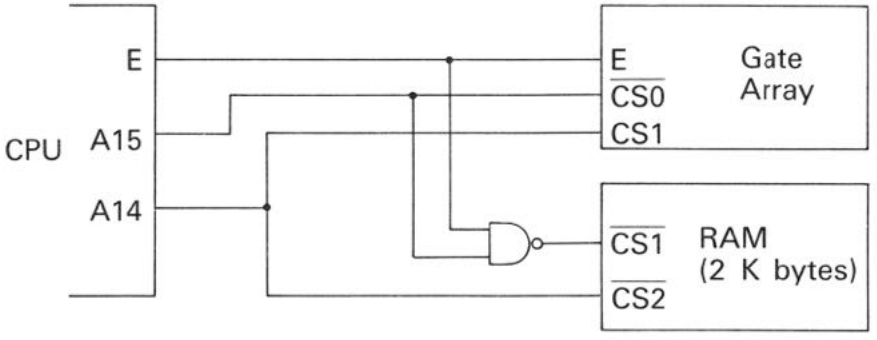


Fig. 6-14

The memory map is as follows:

00H – 1FH: CPU I/O Port
80H – FFH: CPU Internal RAM (128 bytes)
4000H – 4002H: Gate Array
8000H – 87FFH: RAM (2 K bytes)
F000H – FFFFH: CPU Internal ROM (For 4 K byte program)

6-3. Panel PCB

The Panel PCB is connected to the power switch SW501 located on the front of the unit. (Fig. 6-15)
The resistors R502 and R503 are used for discharging large capacitors, coupled between DC+ or +5V and DC− on the power PCB, when the switch is turned off.
LED 501 is the "Low battery" indicator and when the battery is low, the CPU outputs high level at its pin 23 to light the indicator through the invertor.

Circuit Diagram of the Panel PCB

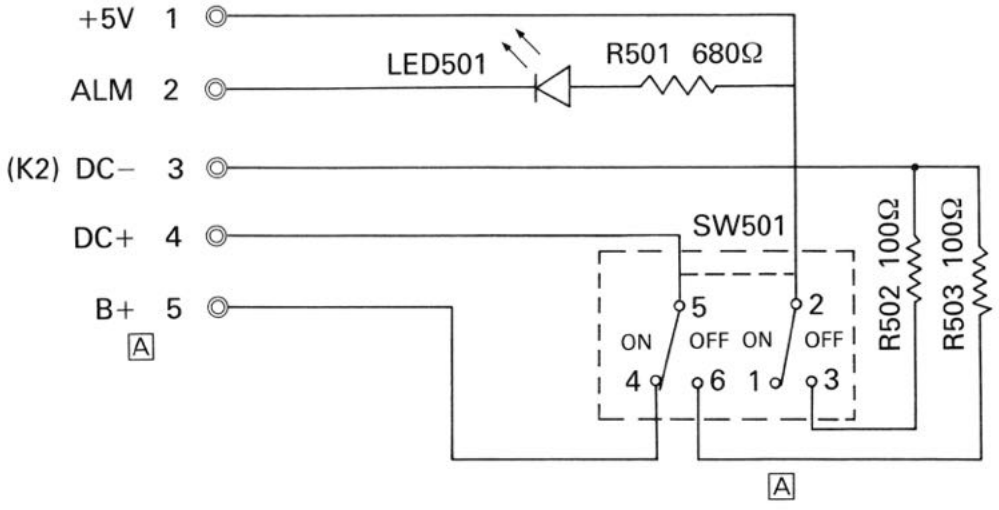


Fig. 6-15

6-4. Power PCB

The power PCB stabilizes the power of +5V supplied from the battery (or adapter) and detects the input voltage. When the input voltage is 4.1V or less, the LBT changes to the low level. When it is 3.5V or less, the EBT changes to the low level. When the output is 0V (zero volt) or the power down signal is input, the power is shut off.
The description of each terminal is as follows:

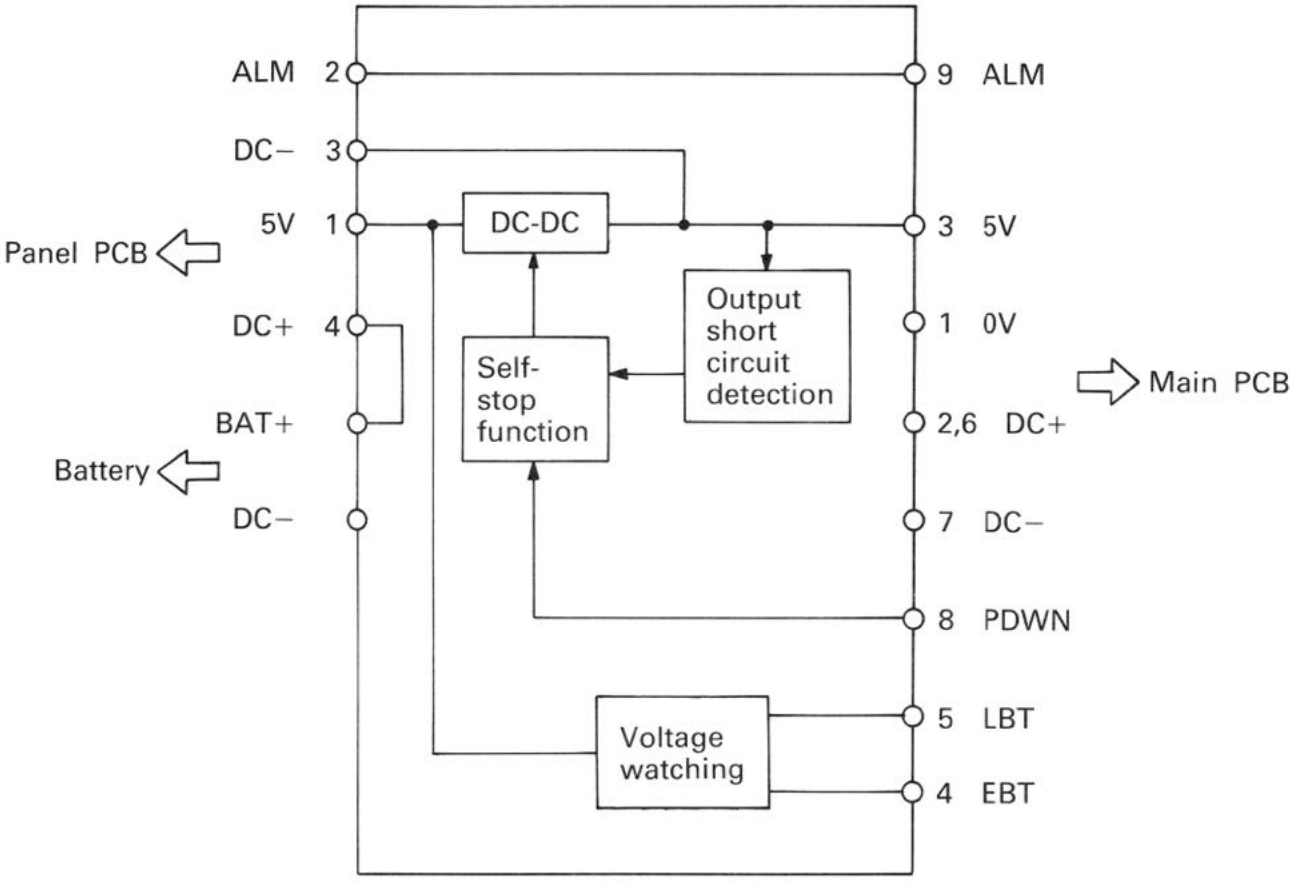


Fig. 6-16

7. EXPLANATION OF BASIC OPERATION

The 8 basic operations of this unit are as follows:

1. Power On/Reset Operation
2. Track 0 Operation
3. Seek Operation
4. Read Operation
5. Write Operation
6. Interface I/O Operation
7. Power Down and Low Battery Operation
8. DC Motor Drive Operation

Each description will be given in detail on the pages following.

7-1. Power On/Reset Operation

Even if the power switch is turned on, the power-supply unit does not receive the power down signal until the operation of the main circuit is fixed. The outputs of the gate array and the CPU are determined when the power reaches level (1). Therefore, the PWD signal is indeterminate when the power voltage is within the range 0V to 3.0V; however, the power is not shut off. Even if the power switch is turned on and off, the disk is not damaged, since the write circuit does not work unless the power voltage is 3.9V or more. When the voltage reaches 4.3V, as explained in the item on the reset circuit, it starts charging the capacitor: the reset signal changes to the high level 75msec. later. When the reset signal goes high, the CPU determines its operation mode as mode 6 (refer to pages 20-22). Then the CPU reads the contents of the internal ROM addressed FFFEH-FFFFH, and the CPU control is passed to the address set forth by the contents of that location. The gate array sets the internal reset state at power on and the initial conditions exist until cancelled by software. These initial conditions are as follows:

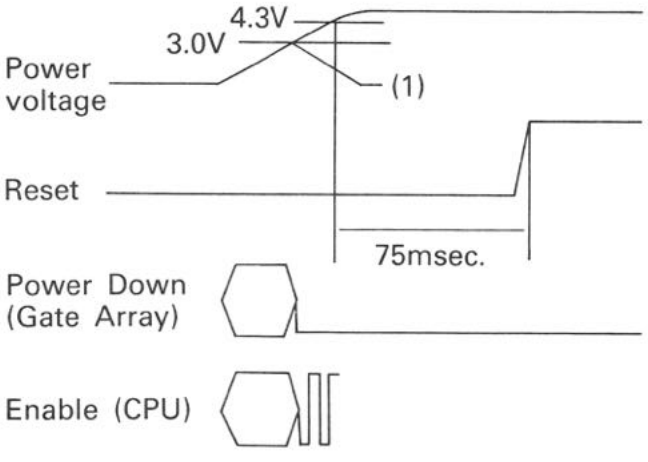
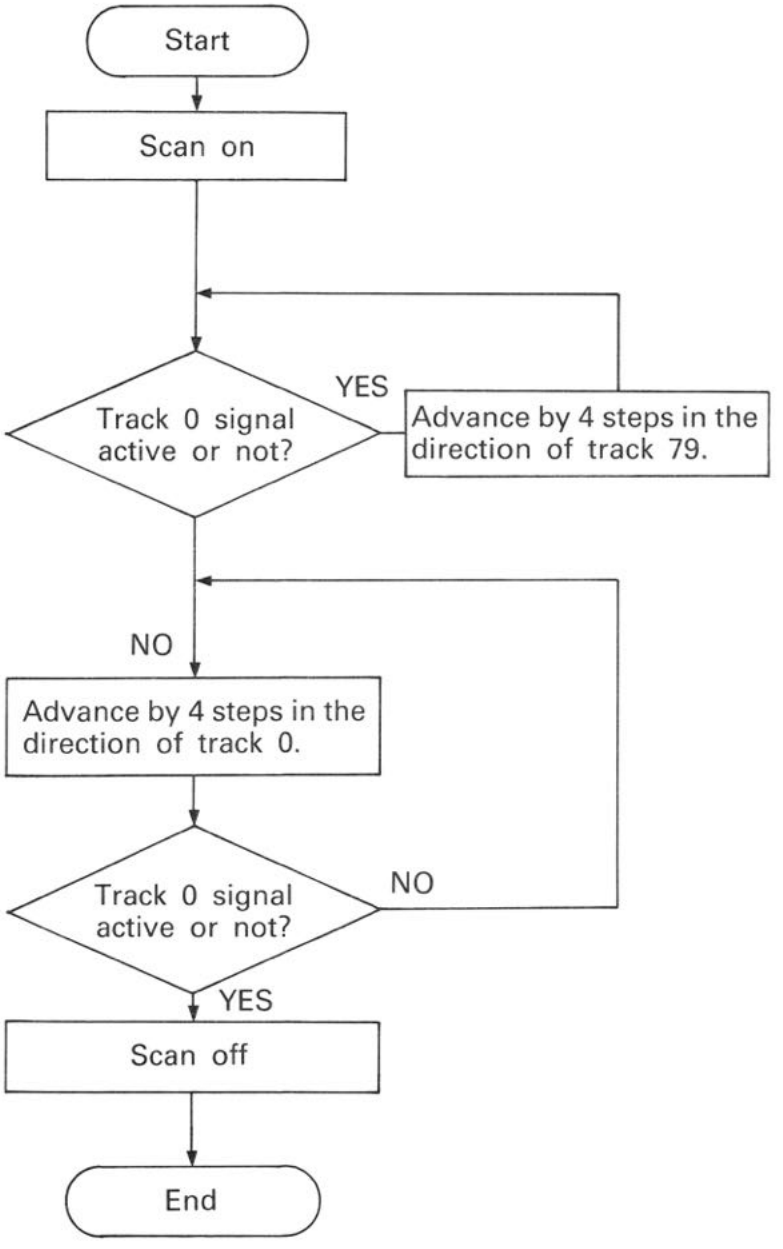


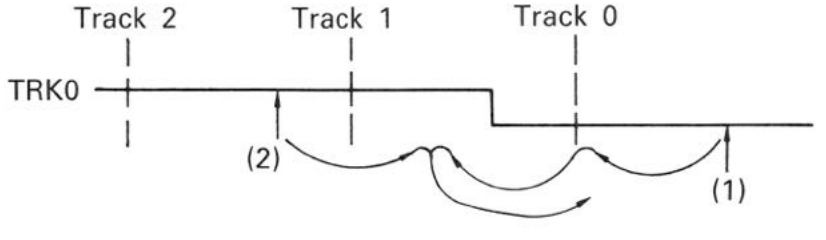
Fig. 7-1

Gate Array	
PWD	Low
WD	Not specified
$\overline{WD}$	Not specified
$\overline{WE}$	Low
STP 0 – 3	High
A0 – A7	Not specified
CLKOUT	High
MTON	Low

7-2. Track 0 Operation



The basic sequence required to move the head to track 0 (zero) is described below. Set P17 of the CPU to the high level at "scan on" and supply the current to the photo-interrupter for sensing the track 0 signal. The track 0 signal varies between the track 0 position and the position where the excitation has the same phase as that of the next track (the position advanced in the direction of track 79 by 4 steps). If the head is located at position (1), the head is moved until TRK0 signal goes high; then it is moved back and stopped when it changes to low. If the head is located at position (2), the head is moved until TRK0 changes to low; the operation stops when P17 of the CPU changes to the low level.



1 Track = 4 Steps

Fig. 7-2

7-3. Seek Operation

The operation to move the head between tracks and the method of phase excitation of the stepping motor are explained below. The distance of one track corresponds to 4 steps of the stepping motor.
Fig. 7-3 shows the waveforms of phase excitation of the gate array.

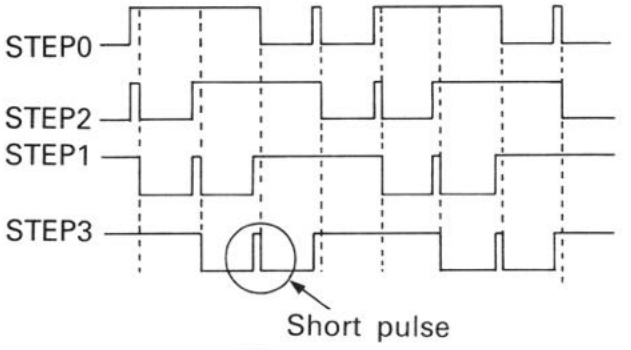


Fig. 7-3

There is a difference between the on-off time and the off-on time of transistors. If the switching operation (on and off) is done without regard to this difference, excessive current flows could damage the transistors.
Therefore, all transistors are immediately turned off, then the next phases are excited to prevent damage. This causes a short pulse to appear as shown in Fig. 7-3. The stepping rate is 100 pps.

Refer to the flowchart in Fig. 7-5.
When power is supplied to this unit, the track 0 operation is performed first; then the current absolute position of the head is stored in RAM. The required number of steps and the direction to the objective track are calculated from the current and objective track positions. By moving in the direction of track 0, the head moves the required number of steps and the excitation at the last stage lasts for 20msec. By moving in the direction of track 79, or by zero steps, the head moves the required number of steps plus one step; then the head moves in the direction of track 0. The excitation at the last stage lasts for 20msec.
The reason for this movement is that the head movement is sometimes unstable in a certain direction because of the head moving mechanism (see the Fig. 7-4). The head is always kept to side A and it is moved in one direction (or in the track-0 direction) to minimize the backlash.

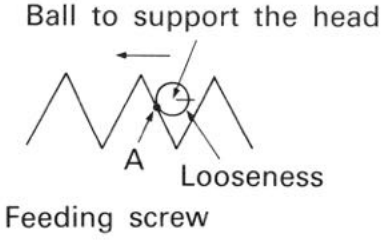


Fig. 7-4

* Direction of Track 0: Outward
Direction of Track 79: Inward

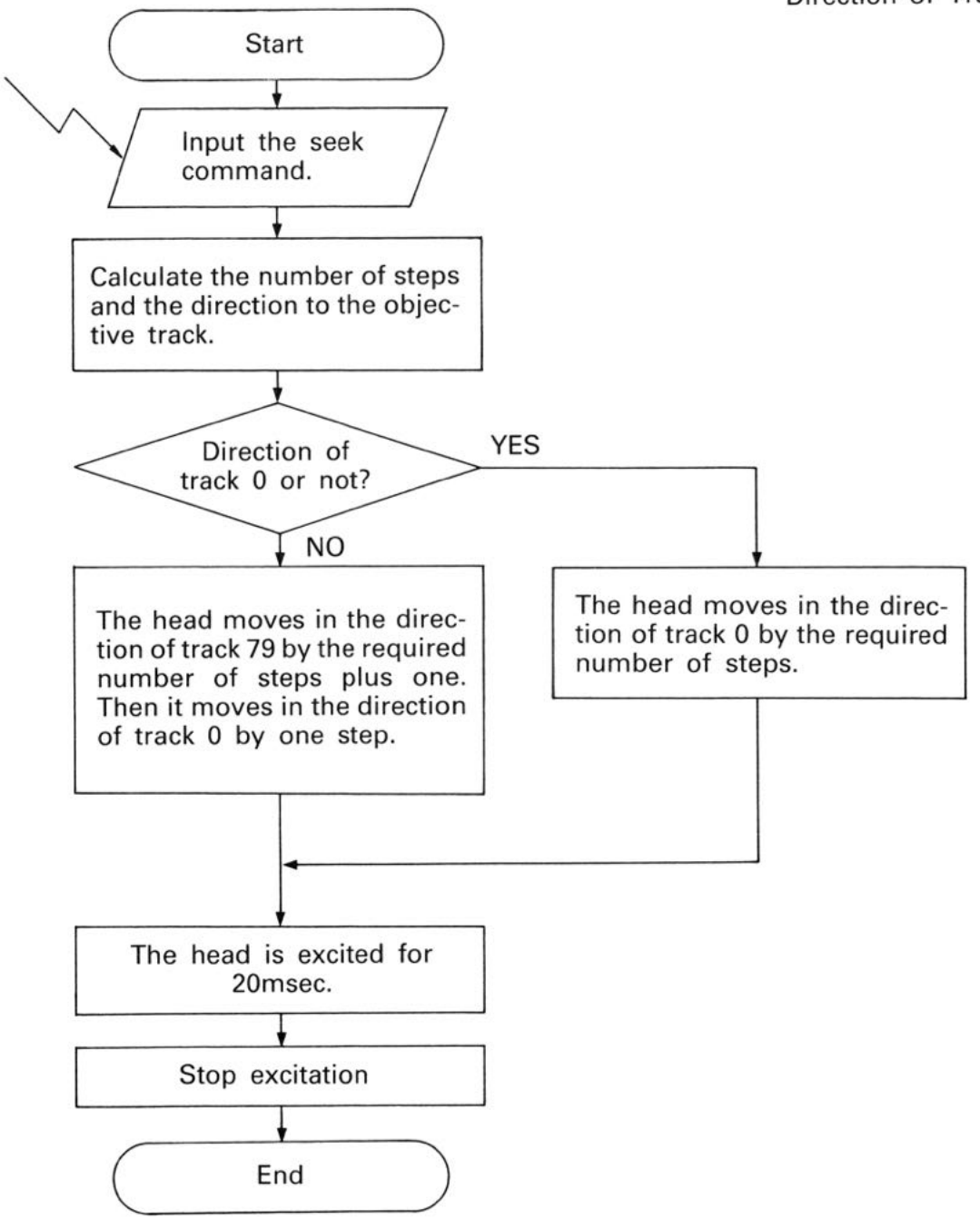
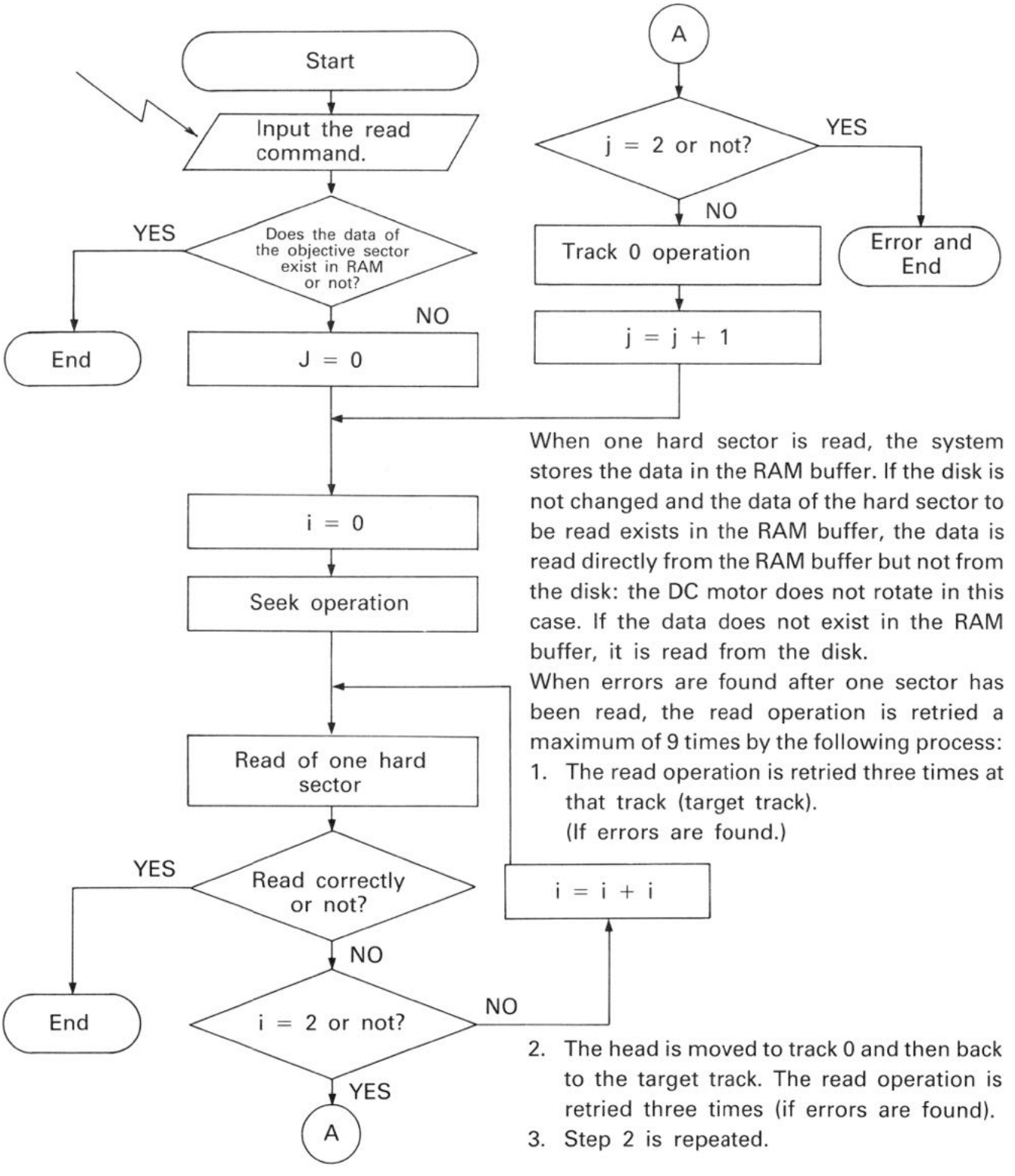


Fig. 7-5

7-4. Read Operation



When one hard sector is read, the system stores the data in the RAM buffer. If the disk is not changed and the data of the hard sector to be read exists in the RAM buffer, the data is read directly from the RAM buffer but not from the disk: the DC motor does not rotate in this case. If the data does not exist in the RAM buffer, it is read from the disk.

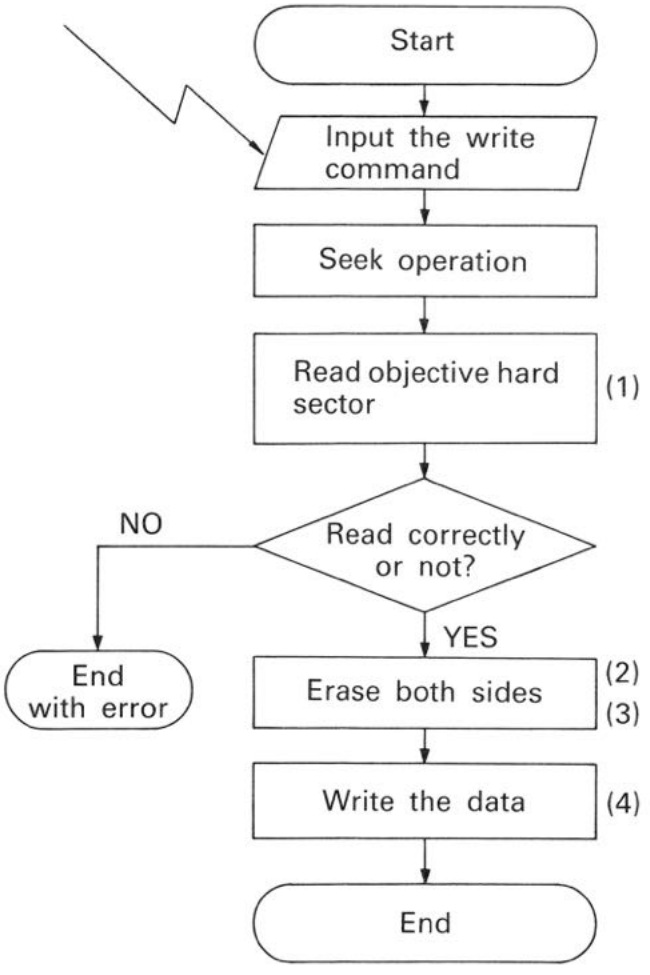
When errors are found after one sector has been read, the read operation is retried a maximum of 9 times by the following process:

1. The read operation is retried three times at that track (target track).
   (If errors are found.)
2. The head is moved to track 0 and then back to the target track. The read operation is retried three times (if errors are found).
3. Step 2 is repeated.

Fig. 7-6

When the error cannot be recovered even after 9 retries, the read operation ends in error. The read operation, however, ends immediately (without retries) when the disk is not set or unrecoverable (fatal) errors are found – for example, when the index signal cannot be detected or when the track 0 signal cannot be detected.

7-5. Write Operation



Because this disk drive is not equipped with an erase head, the erase operation is done by the read/write head. When the write command is received, the objective sector is sought and read. At this stage, the ID of the disk is checked to determine whether the head arrived at the objective track. If the objective sector cannot be read even after 12 retries, the write operation ends with an error condition. Otherwise, the head moves one step in the direction of track 79, as shown in Fig. 7-7(2), to erase the objective hard sector. In erasing the data, the signals WD and $\overline{WD}$ are kept high and low or low and high, respectively. Then the head moves two steps, as shown by (3), to erase the other side of the track. The head eventually moves one step to write the data on the objective track.

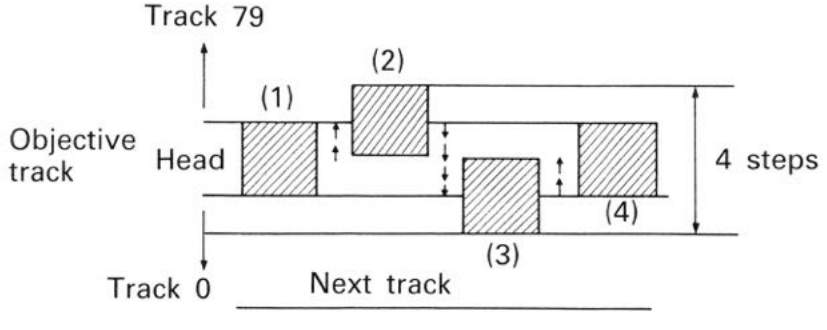


Fig. 7-7

7-6. Interface I/O Operation (The signal names of the host are used in the following.)

When the power is turned on, the CPU sets the DSR active within 500msec. The standard clock for the serial interface is stabilized during this time, while CTS remains low. Then the track 0 operation is performed. When DTR and RTS are active, CTS is ready to accept the command.

Power On Stage

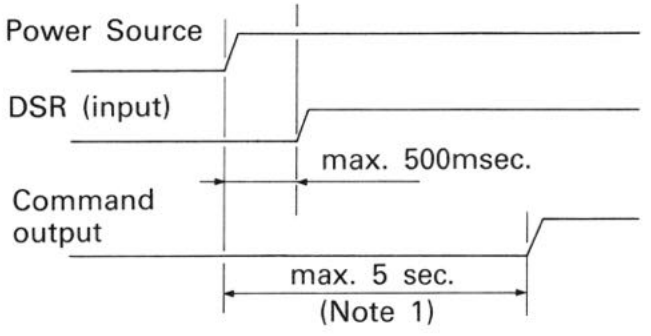


Fig. 7-8

Note 1: The DTR and the RTS should already be active. The command should not be output when they are not active.

In the single drive mode, the 4 control lines RTS, CTS, DTR and DSR are used in principle. It is possible to input and output the data without judging CTS as long as RTS and the DTR are kept active. In operation mode, the 2 control lines DTR and DSR are used. Fig. 7-9 shows the timing of the FDC mode and the TEST mode.
The CPU checks RTS 25msec. after DTR becomes active. If RTS is judged active, CTS is activated. The host outputs the command after CTS becomes active. If the host does not refer to the CTS signal, the host should output the command at least 25msec. after DTR is activated.

Output Timing of DTR and Command

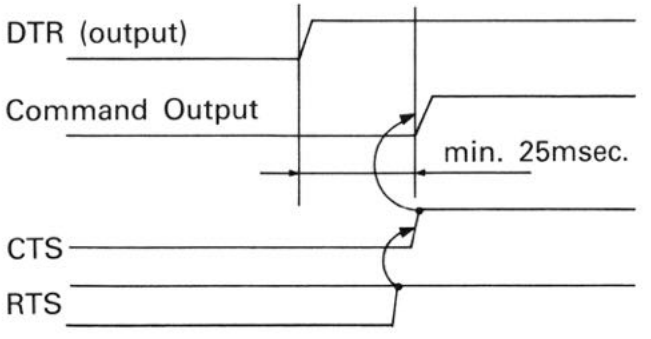


Fig. 7-9

Fig. 7-10 shows the data output operation. DTR and DSR are in the active condition. When RTS becomes active, the disk drive detects it and sets CTS active.

(1) The host activates the RTS line as data is requested. The disk drive watches the RTS line. The drive activates the CTS line when it detects that RTS is active.
(2) The host transmits data after checking that the CTS line is active.
(3) The disk drive receives data and makes the CTS line inactive.
(4) The host makes the RTS line inactive to see that the CTS line is inactive.

Note: The disk drive does not watch the RTS line in (4), The host can fail to make the RTS line inactive when it transmits a series of data.

Data Output

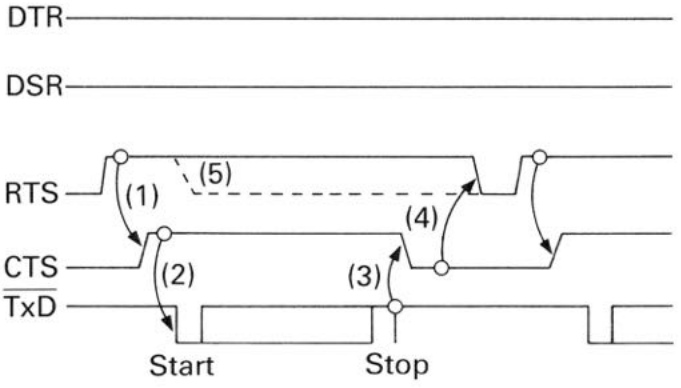


Fig. 7-10

When DTR is active, the disk drive decides which data can be output and outputs it. The start bit of the following byte should be input into the host within a maximum of 30 usec. after the stop bit of the preceding byte is input. Therefore, the data should be input less than every 30+(10/Baud rate) x 10^6 [usec].

Data Input

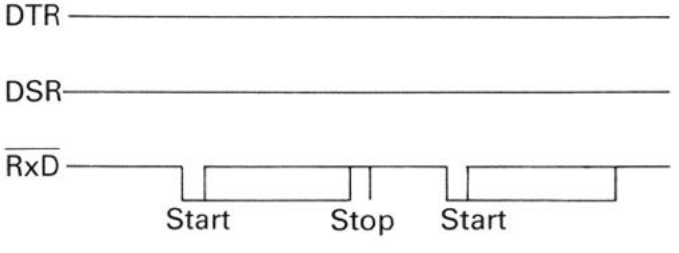


Fig. 7-11

Fig. 7-12 shows the timing of the serial interface in operation mode.
After the host finds DSR is active, it outputs the data. The maximum speed of transmission is 19200 bps. It takes 200msec. for the host to stabilize the $\overline{T \times D}$ line after DTR becomes active; the host outputs the data 200msec. later.

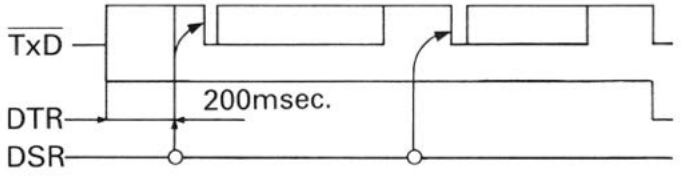
The drive uses only DTR and DSR control lines for serial communication.

On data output, after DTR is activated, the drive knows DSR is active, waits min. 200msec. and sends the data.(a)

On data input, if DTR is active, the drive sends items of data one after another.(b)
During input of the data, the host must make DTR active.

Serial Interface Timing

(a) Data Output



(b) Data Input

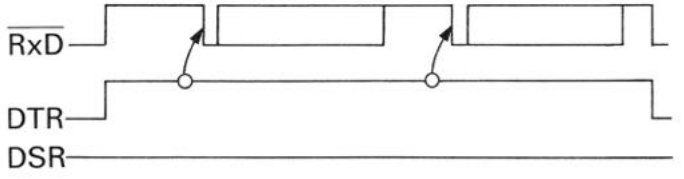
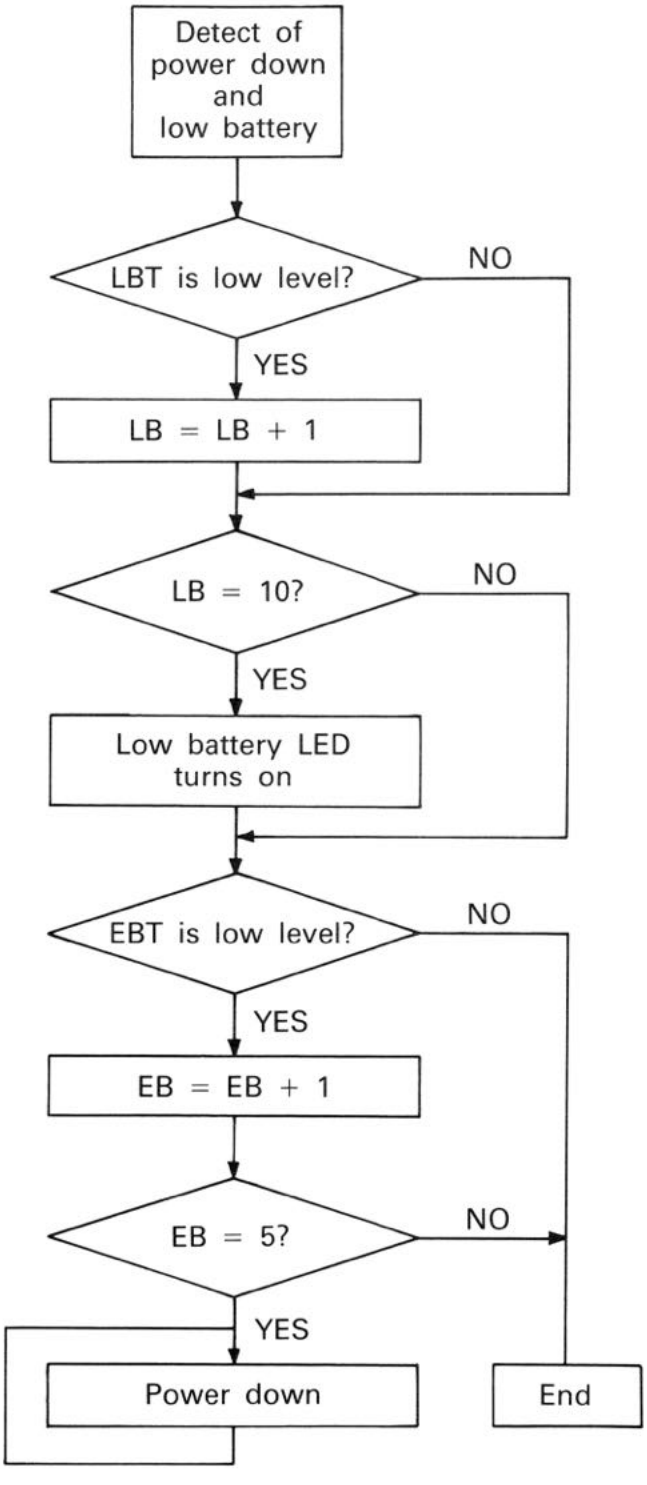


Fig. 7-12

7-7. Power-down and Low Battery Operation



To detect a low battery condition, the drive checks LBT signal at about 100ms intervals. If LBT becomes low level more than 10 times, the CPU sets P14 high level to turn on the low battery LED.

On power-down, the drive checks the EBT signal at about 100ms intervals. If EBT becomes low level more than 5 times, the CPU sets the PWD terminal of the gate array to high level to cut off the DC-DC power supply circuit.

The accumulated times that the LBT and EBT are initialized when the drive is powered on/reset.

7-8. DC Motor Drive Operation

The DC motor is turned on when the read/write operations are actually performed. Once turned on, the motor will continue to run for about 3 sec. after the operation is finished.
When operations are performed continuously, one right after another, there is no need to wait for the rising time of the motor (0.8 sec) each time.
That's the reason the motor continues to run for 3 sec. after one operation is finished.

8. STANDARD MAINTENANCE

Exerciser Portable Computer and Adjusting Tools

(1) Necessary Apparatus

a. Model 100/Tandy 200
b. CE (alignment) disk
c. Oscilloscope (2 channels)
d. Appropriate drive diagnostic
e. Soldering iron and solder
f. Normal disk
g. Frequency counter

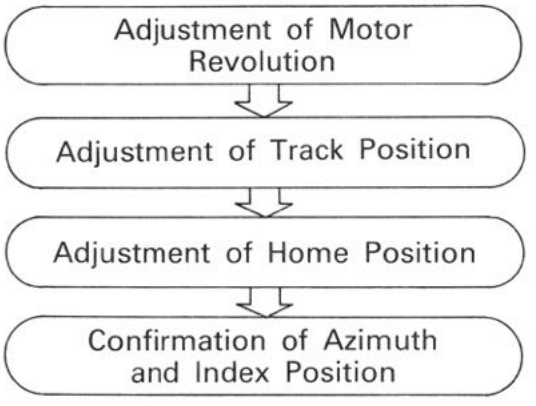
(2) Main PCB checkpoints (Refer to Fig. 10-2 on page 52)

1) CH102 or CH103 ..... Waveform output signal of read/write head
2) CH120 ..... Index signal
3) CH121 ..... Track 00 signal
4) 0V ..... Ground
5) Switch Part

To observe each signal on an oscilloscope, the ground of the probe should be 0V and the probes should be connected with the checkpoints of each signal.

(3) Adjustment with Model 100

Place tape which is impervious to light over the smaller cut of the encoder.



Adjustment flowchart

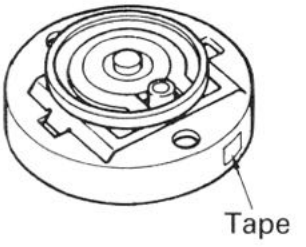
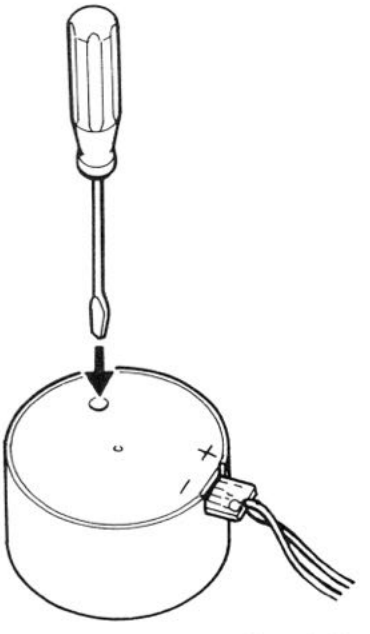


Fig. 8-1

1. Adjust the Motor Speed

   Connect the ground of the probe of the counter to 0V shown in Fig. 10-2 and the hot lead of the probe to the index signal of CH120.

   Insert a screwdriver into that part of the DC motor indicated by the arrow. (See Fig. 8-2.)
   Turn the screwdriver so that the value of the counter is within the range 4.975 Hz to 5 Hz. Attach the cover after the adjustment.



DC Motor **Fig. 8-2**

2. Connect the ground lead of the CH1 probe of the oscilloscope to 0V (Ground) shown in Fig. 10-2. Connect the hot lead of the CH1 probe to the index signal of CH120. Connect the hot lead of the CH2 probe to the waveform output of CH102 or CH103. Set the time interval of the oscilloscope to 20msec/DIV. The CH1 should be 1V/DIV and the CH2 should be 100mV/DIV. The triggering is done at CH1 according to the index.
3. Eject the normal disk and insert the CE alignment disk.

4. Move the head to track 00. Check that the waveform of the CH2 appears on the oscilloscope.

   If the waveform does not appear, press 0 after moving the photo-interrupter for track 00 repeatedly until it appears.

5. Adjust the track position.

   a. After moving the head to track 40 where the cat's eye is recorded, turn the stepping motor for the head feed by hand so that 2 outputs just after the indexes are almost equal to each other ($V_{1P-P} = V_{2P-P}$) as shown in Fig. 8-3.
   b. Move the head to track 00 and then back to track 40 to verify the cat's eye pattern is still present. Readjust as necessary.

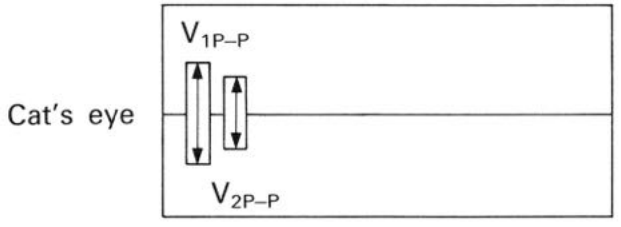


Fig. 8-3

Note: It is necessary to remove the adhesive for readjustment since the adjusted stepping motor is glued.

6. Adjust the home position (Track 00)

   Connect the CH1 probe of the oscilloscope to the track 00 signal of CH121. Check that the signal is about 0V (zero volt). Then move the head inward, step by step. The signal should become 5V between track 00 and track 3. If the signal does not become 5V by the time track 3 is reached, move the photo-interrupter outward a little and start again.

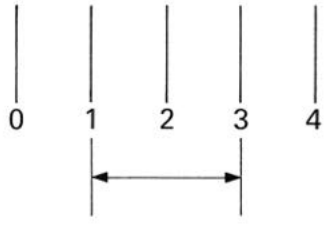


Fig. 8-4

7. Repeat procedure 6. once again. Then, using instant bonding glue, fix the photo-interrupter to the chassis.
8. Complete the adjustment.
9. Be sure to inspect the unit according to the procedure in subsection (4).

(4) Inspection

1. Connect the ground lead of the oscilloscope to 0V, the CH1 probe to the CH120, and the CH2 probe to CH102 or CH103.
   Connect the ground lead of the Frequency counter to the signal of CH120.
2. Check that the screen is as shown in subsection (3).
   Then insert the CE disk.
3. Move the head to track 40.
   Measure the output of the cat's eye.
   The ratio of V_{2p-p} is within the range 0.67 to 1.50.

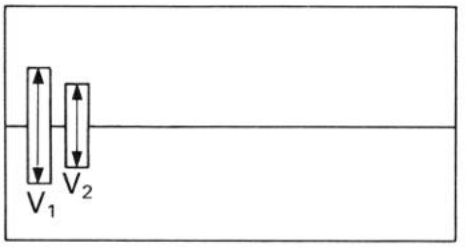


Fig. 8-5

When the waveform appears on the oscilloscope as shown in Fig. 8-5, measure the first V1 and V2.

4. Move the head to Track 74 and measure the azimuth.
   (Set the azimuth within ±18'.)

   ± 0' when V3 = V6 < V4 = V5
   +18' when V6 = V3 = V4 < V5
   −18' when V3 < V5 = V6 < V4

   Therefore,

   ±18' when V3 ≦ V4 and V5 ≧ V6

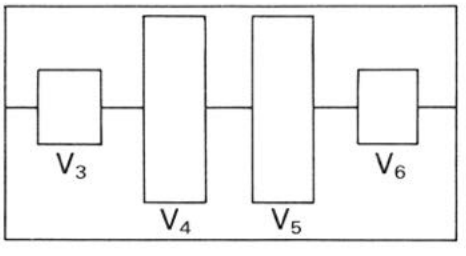


Fig. 8-6

5. Measure the index position. (Within 5 ± 1ms)

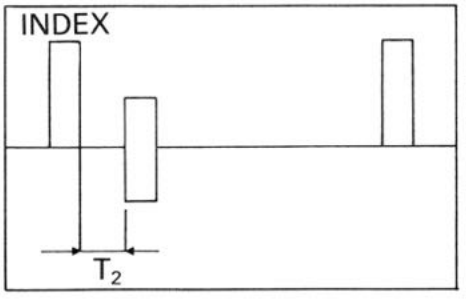


Fig. 8-7

6. Move the head to track 79.
   Measure the revolution in the same way as mentioned in subsection (3).
   (298.5 to 300 RPM)

7. Remove the CE disk and insert a normal disk.

8. Measure the resolution of the head at track 79.
   Write a 1F pattern and measure the Vmax as shown in Fig. 8-8 (V_{1F}).
   Write the 2F and measure the Vmax as shown in Fig. 8-8 (V_{2F}).
   The resolution is calculated by the following formula:

$$\frac{V2F}{V1F} \times 100\%$$ (The output of 2F should be more than 100 mV.)

   The resolution must be more than 60%.

Measure the modulation.
   Write 2F data on a disk when the waveform appears on the oscilloscope as shown below.

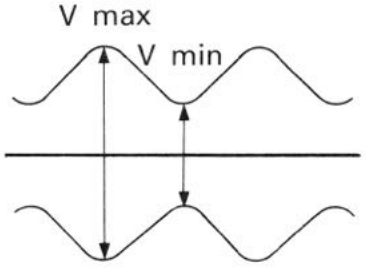


Fig. 8-8

   Measure the Vmax and the Vmin. And calculate the modulation by the following formula:

$$\frac{V\ max - V\ min}{V\ max + V\ min} \times 100\%$$

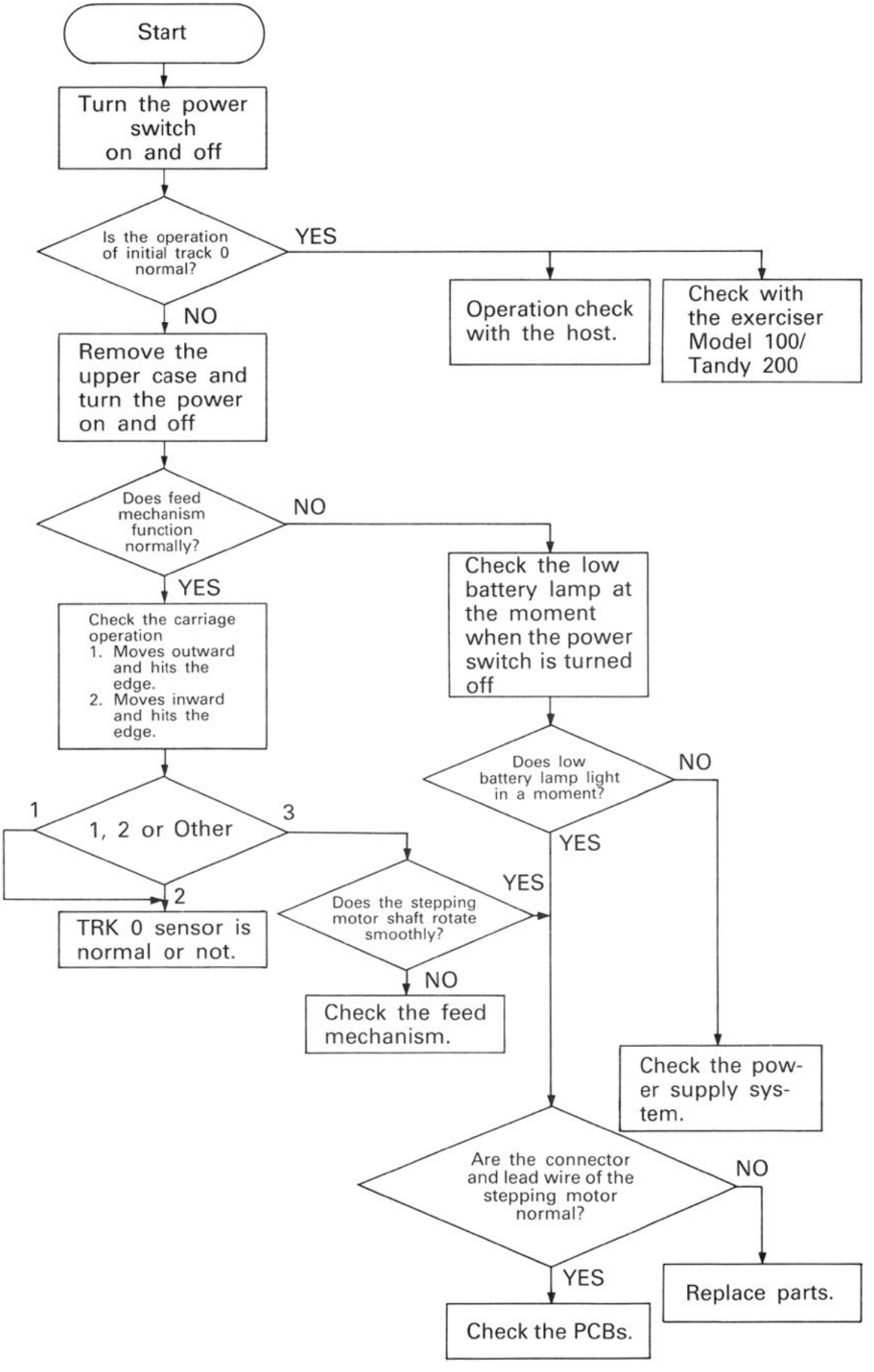
   And measure the revolution from the counter.
   Ensure the value of modulation is within 10%.

9. Move the head to track 00.
   Write 1F and measure the modulation. Ensure that the value of modulation is within 10%.

10. The inspection is completed.

IMPORTANT NOTE:
   Be sure to remove the tape which covers the small cut of the encoder.

9. TROUBLESHOOTING



10. P.C. BOARD VIEWS

Main PCB Top View

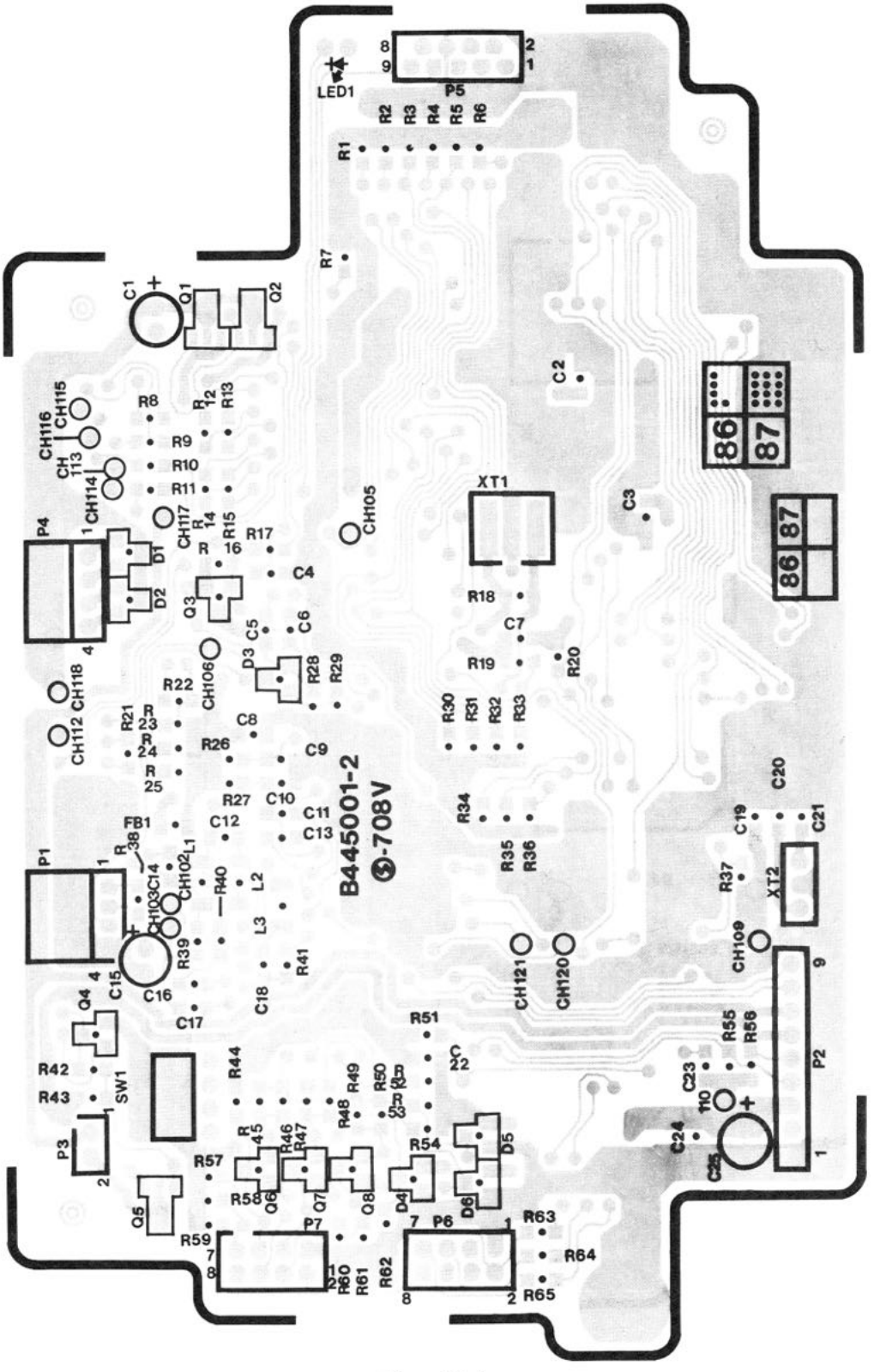


Fig. 10-1

Main PCB Bottom View

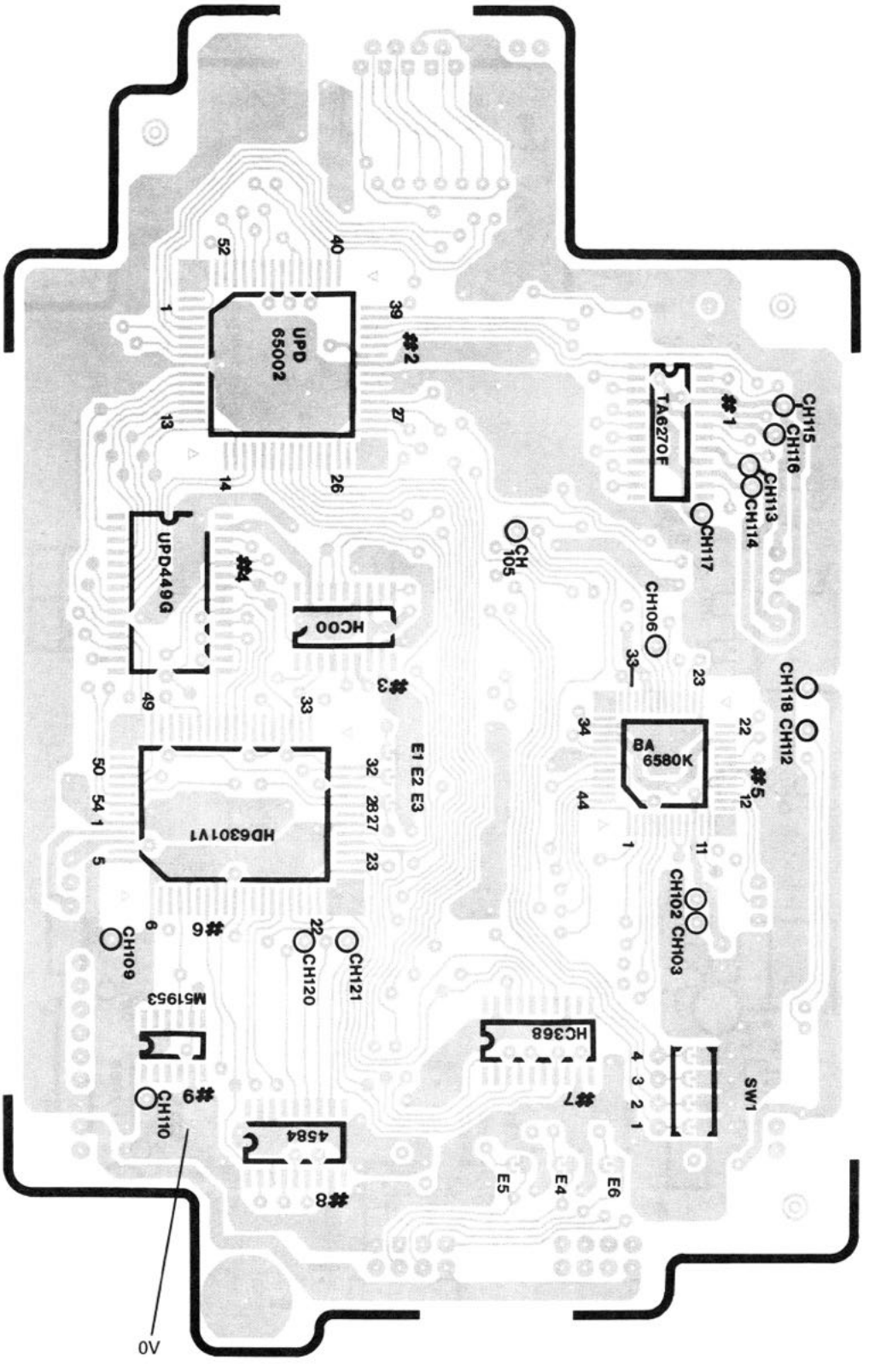


Fig. 10-2

Power PCB Top View

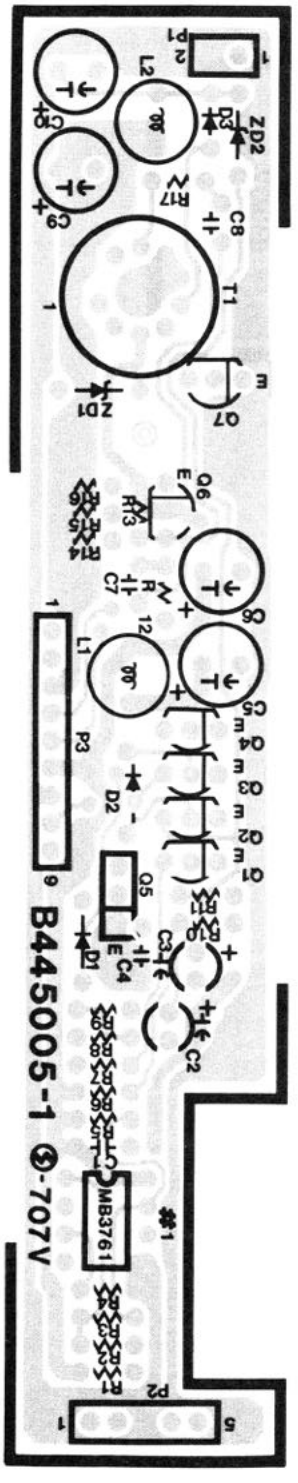


Fig. 10-3

Power PCB Bottom View

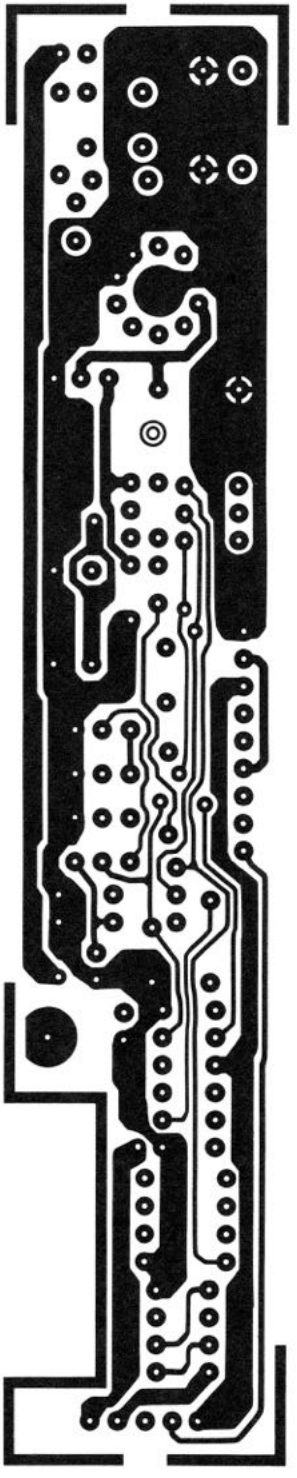


Fig. 10-4

Panel PCB Top View

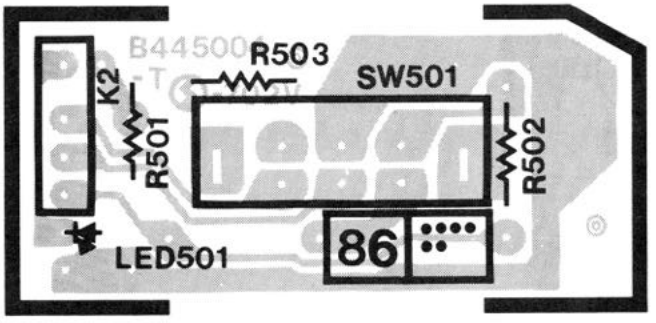


Fig. 10-5

11. EXPLODED VIEWS/PARTS LISTS

11-1. HOUSING PARTS

HOUSING PARTS EXPLODED VIEW

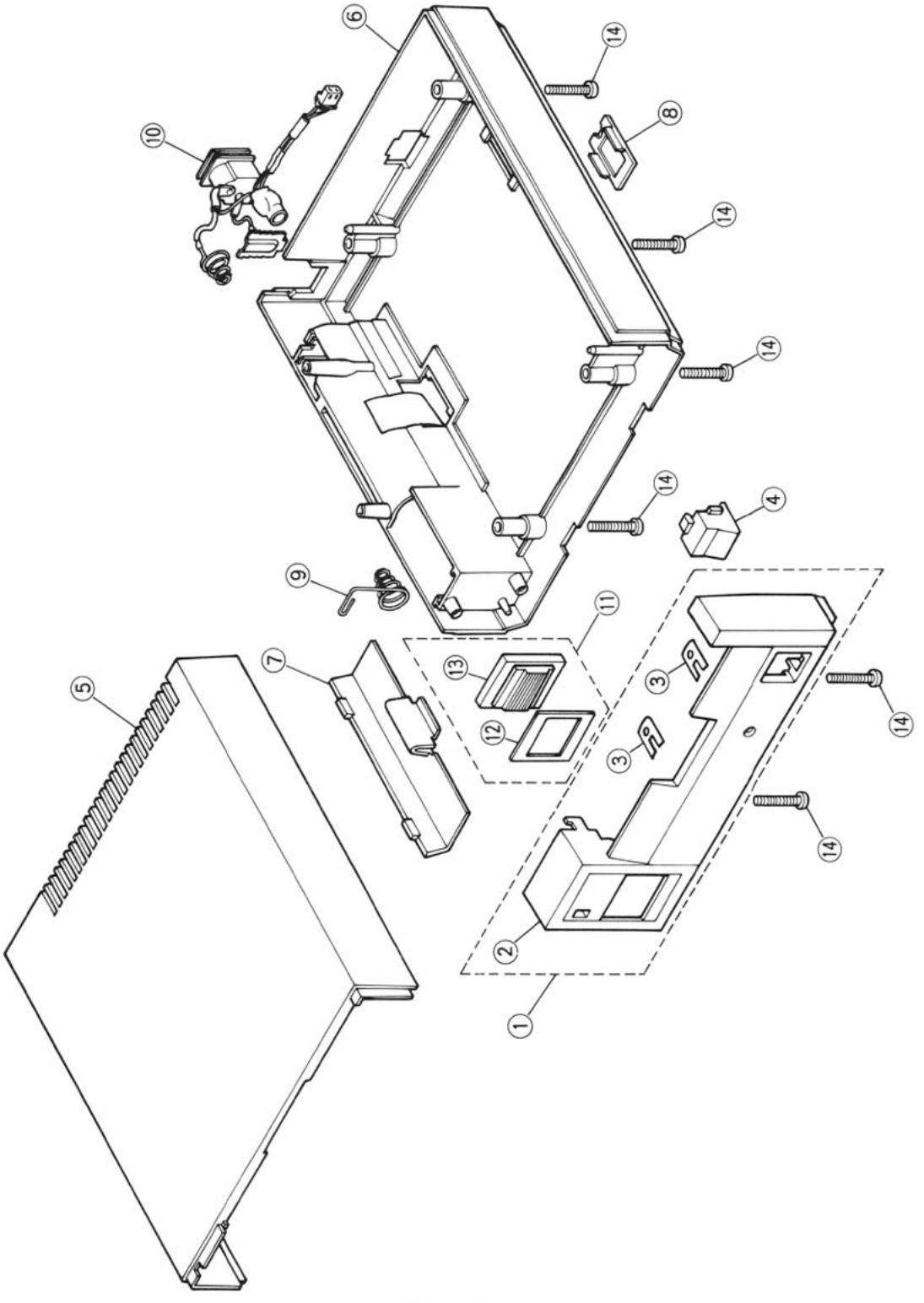


Fig. 11-1

HOUSING PARTS LIST

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
1	Bezel ass'y, Front	AZ0131	W01039001
2	Front bezel		W01040001
3	Washer A type		W00349000
4	Eject button	AK0347	W00084002
5	Case ass'y, Upper	AZ3959	W00085002
6	Case ass'y, Lower	AZ3960	W80003001
7	Battery case cover	ADB0261	W00090002
8	DIP switch cover	AHC0126	W00091002
9	Spring, Battery coil	AB0625	W00095001
10	Battery contact ass'y	AB0626	W00102001
11	Cover ass'y, Power switch	AHC0382	W80096001
12	Switch sheet		W00099001
13	Cover, Power switch	AHC0128	W00100002
14	Screw, M3x16, pan head	HD2066	062301606

11-2. DRIVE MECHANISM

DRIVE MECHANISM EXPLODED VIEW

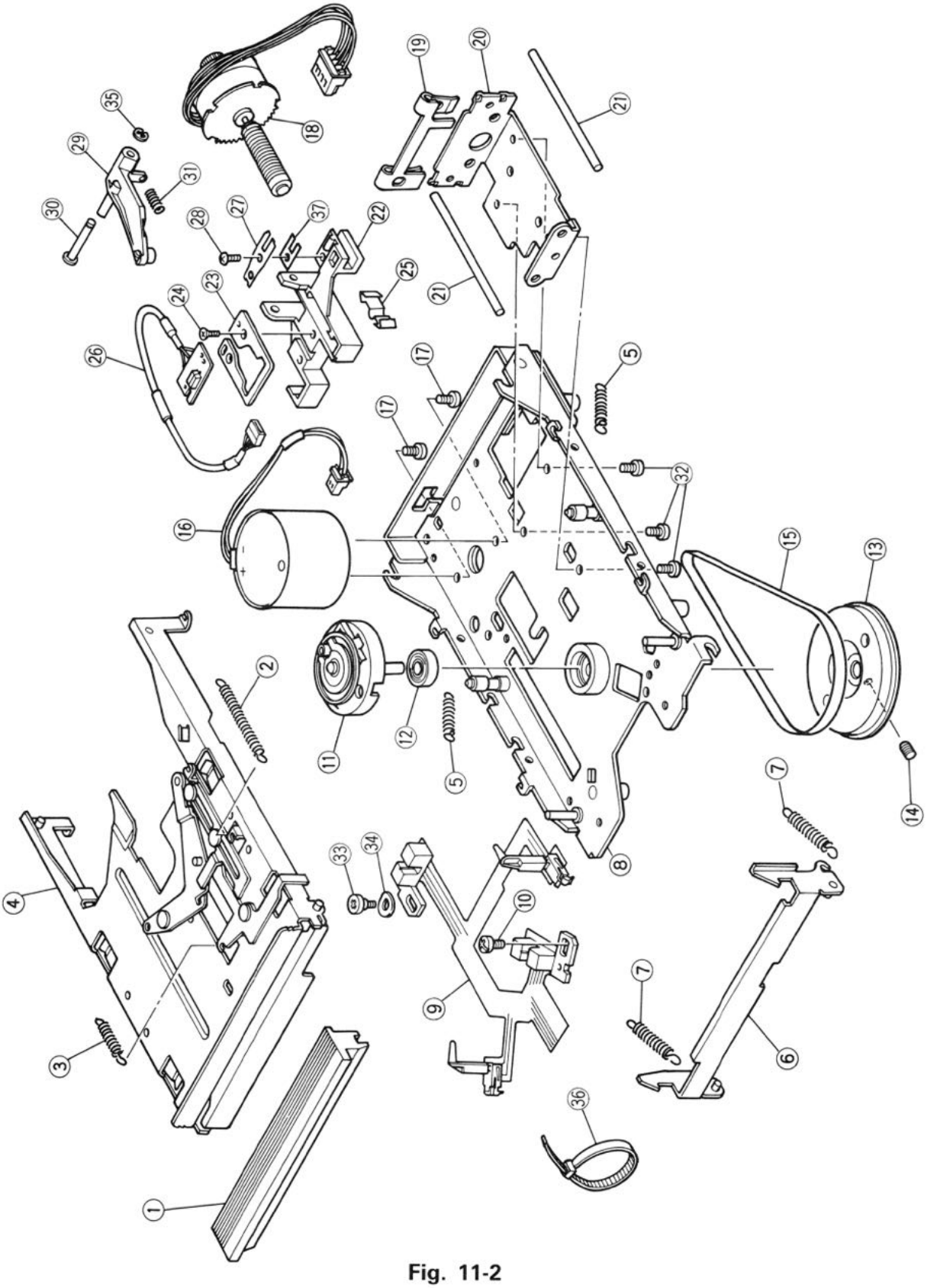


Fig. 11-2

DRIVE MECHANISM PARTS LIST

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
1	Disk in/out bar	ART0108	W00003002
2	Spring, Loading plate	ARB0500	W00004001
3	Spring, Loading nail	ARB0501	W00005001
4	Disk holder ass'y	ART0109	W00006001
5	Spring, Disk holder	ARB0502	W00017001
6	Clamp plate ass'y	ART0110	W00025001
7	Spring, Clamp	ARB0503	W00027001
8	Chassis ass'y		W00019001
9	Sensor cable ass'y	AW1025	W00028001
10	Screw, M3x4, binding head	AHD1045	060300406
11	Disk shaft ass'y	ART0111	W00031001
12	Ball bearing	AHC0121	W00041001
13	Disk pulley	ARA0029	W00042001
14	Set screw, M3x5, with hexagon socket	AHD1046	014300532
15	Urethane belt UR-70	AB6382	W00043001
16	Motor ass'y, DC 0.6W	AM4047	W01072001
17	Screw, M2.6x4,6, with claw	AHD1047	W00471001
18	Step motor whole ass'y	AM4048	W01045001
19	Spring, Motor holding	ARB0014	W00055000
20	Plate, Motor holding	ART0290	W00057001
21	Shaft, lead table	ART0112	W00059001
22	Lead table ass'y	ART0113	W00060001
23	Head holder	ART0114	W00063000
24	Screw, M2x4, pan head	AHD1105	061020506
25	Spring, Shaft holding plate	ARB0505	W00064000
26	Magnetic head ass'y with shield ring	AH4009	W80045001
27	Lead spring ass'y	ARB0506	W00065001
28	Screw, M2x3, truss head	AHD1049	008020316
29	Pad arm ass'y	ART0115	W00075001
30	Pad arm shaft ass'y	ART0116	W00109001
31	Spring, pad arm	ARB0507	W00101001
32	Screw, M2.6x4.6, with claw	AHD1047	W00471001
33	Screw 2.6, flat head	AHD1051	W00179001
34	Washer	AHD8031	W00198000
35	Snap ring E2	AHE0066	048020346
36	Binder #2		411746001
37	Spacer	AHC0377	W0103800

11-3. ACCESSORIES

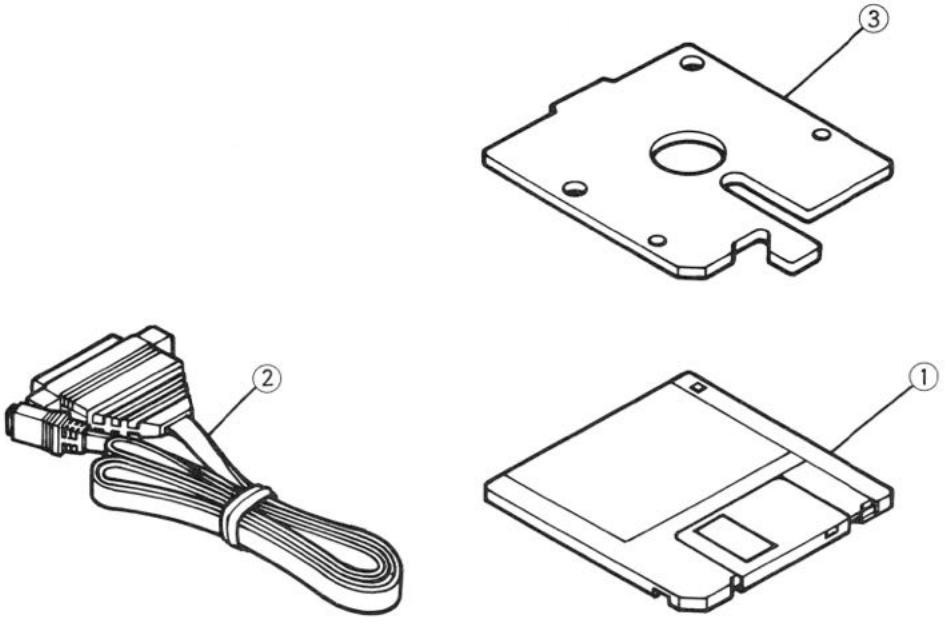


Fig. 11-3

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
1	Diskette, Utility	AXX2056	W01041001
2	Cable, Serial	AW0042	W01042001
3	Sheet, Head protect	AHC0127	W00463001

11-4. ELECTRONIC/ELECTRIC PARTS

ELECTRONIC/ELECTRIC PARTS EXPLODED VIEW

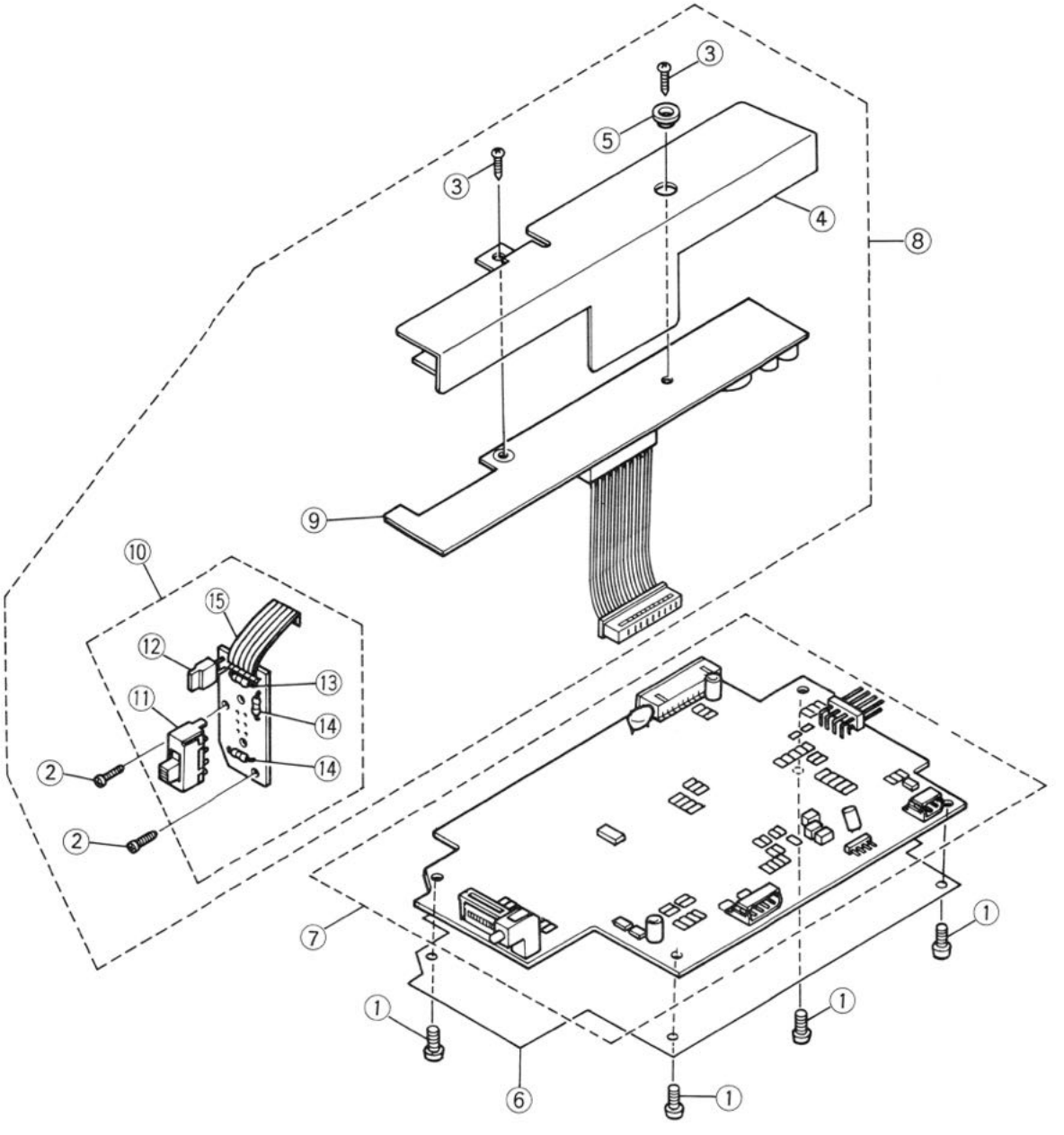


Fig. 11-4

PCB INSTALLATION SECTION

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
1	Screw, M26x4, binding head	AHD1106	060260406
2	Screw, M2x6, pan head	HD2009	037200616
3	Screw, M2x8, pan head	HD2011	037200816
4	Plate, Upper shield	ART0291	W00857001
5	Collar, Shield plastic	AHC0378	W00181000
6	Plate, Lower shield	ART0292	W01034001

MAIN PCB ASSEMBLY

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
7	PCB ass'y, Main	XB1504	W00752001
	CAPACITORS		
C1	Capacitor, Electrolytic, 22μF, ±20%, 16V, USA1H220MCA	CC226MDCA	Y42202702
C2, 3	Capacitor, Ceramic, 0.1μF, +80%, −20%, 25V GR42-6F104Z25	CD104KFBC	Y81042406
C4	Not used		
C5, 6	Capacitor, Ceramic 220pF, ±10%, 50V, GR42-6CH221K50	CD221KJBC	Y72211116
C7, 8	Capacitor, Ceramic 0.1μF, +80%, −20%, 25V GR42-6F104Z25	CD104KFBC	Y81042406
C9	Capacitor, Ceramic, 33pF, ±10%, 50V, GR42-6CH330K50	CD330JJBC	Y73301116
C10	Capacitor, Ceramic 220pF, ±10%, 50V, GR42-6CH221K50	CD221KJBC	Y72211116
C11	Capacitor, Ceramic, 0.1μF, +80%, −20%, 25V GR42-6F104Z25	CD104KFBC	Y81042406
C12	Capacitor, Ceramic, 270pF, ±10%, 50V GR42-6CH271K50	CD271KJBC	Y72711116
C13	Capacitor, Ceramic, 0.1μF, +80%, −20%, 25V GR42-6F104Z25	CD104KFBC	Y81042406
C14	Capacitor, Ceramic, 120pF, ±10%, 50V, GR42-6CH121K50	CD121JJBC	Y71211116
C15	Capacitor, Electrolytic, 1μF, ±20%, 50V, USA1H010MCA	CC105MJBA	Y41095702
C16, 17	Capacitor, Ceramic, 0.1μF, +80%, −20%, 25V, GR42-6F104Z25	CD104KFBC	Y81042406
C18	Capacitor, Ceramic, 1000pF, ±10%, 50V, GR42-6CH102K50	CD102KJBC	Y71021116

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
C19	Capacitor, Ceramic, 0.1μF, +80%, −20%, 25V GR42-6F104Z25	CD104KFBC	Y81042406
C20, 21	Not used		
C22	Capacitor, Ceramic 0.1μF, +80%, −20%, 25V GR42-6F104Z25	CD104KFBC	Y81042406
C23	Capacitor, Ceramic, 0.22μF, +80%, −20%, 25V GR42-6F224Z25	CD224ZFBC	Y82242406
C24	Not used		
C25	Capacitor, Electrolytic, 22μF, ±20%, 16V, USA1H220MCA	CC226MDCA	Y42202702
C26	Capacitor, Ceramic, 33pF, ±10%, 50V, RPE122CH330K50	CC330KJBC	Y23300021
	CONNECTORS		
P1	Connector, A4-4PA-2DS	AJ7011	W00356001
P2	Connector, 5484-09AX	AJ5134	W00760001
P3	Connector, 5268-02A	AJ1034	412412001
P4	Connector, 5268-04A	AJ1033	W00127001
P5	Connector, 5597-09CPB	AJ1035	W00130001
P6	Connector, RF-H081SD1114	AJ5133	W00856001
	DIODES		
D1, 2	Diode 1SS184, Silicon	DX0771	230236000
D3	Diode 1SS181, Silicon	DC0465	U40271000
D4, 5, 6	Diode 1SS226, Silicon	DX0375	W00122001
LED1	LED lamp ass'y	AL1012	W00150001
	ICs		
#1	IC, TA6270F, Stepper driver	MX6125	W00753001
#2	LSI, μPD65002G, C-MOS, Gate array	MX5026	W00113001
#3	IC, TC74HC00F, C-MOS, Quad 2-input NAND	MX6138	093600000
#4	LSI, HM6117FP4, C-MOS, 2KB S-RAM	MX6385	W00754001
#5	IC, BA6580K, Read/Write Amplifier	MX6512	W00704000
#6	LSI, HD6301V1F23F, C-MOS, 8bit CPU	MX6549	W00751001
#7	IC, TC74HC368F, C-MOS, Hex 3-State Bus Inverters	MX7055	093600368

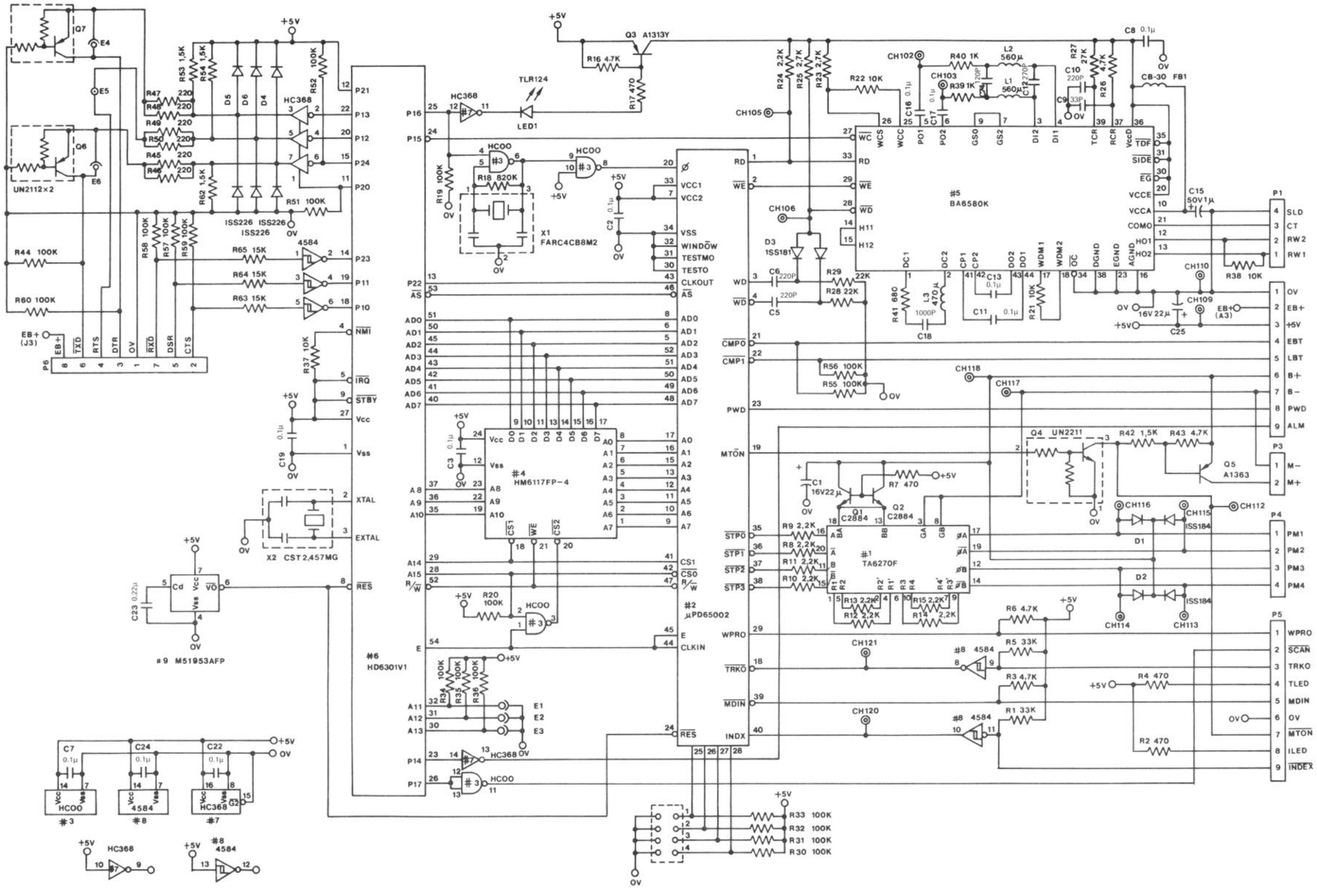
REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
#8	IC, TC4584BF, C-MOS Hex Schmitt Trigger Inverters	MX5037	W00116001
#9	IC, M51953AFP, Voltage detector	MX7484	U80612000
	RESISTORS		
R1	Resistor, MCR18-333EJ, metal, 33KΩ, 0.125W, 5%	ND0324EBD	094333225
R2	Resistor, MCR18-471EJ, metal, 470Ω, 0.125W, 5%	ND0169EBD	094471225
R3	Resistor, MCR18-472EJ, metal, 4.7KΩ, 0.125W, 5%	ND0247EBD	094472225
R4	Resistor, MCR18-471EJ, metal, 470Ω, 0.125W, 5%	ND0169EBD	094471225
R5	Resistor, MCR18-333EJ, metal, 33KΩ, 0.125W, 5%	ND0324EBD	094333225
R6	Resistor, MCR18-472EJ, metal, 4.7KΩ, 0.125W, 5%	ND0247EBD	094472225
R7	Resistor, MCR18-681EJ, metal, 680Ω, 0.125W, 5%	ND0183EBD	094681225
R8-15	Resistor, MCR18-222EJ, metal, 2.2KΩ, 0.125W, 5%	ND0216EBD	094222225
R16	Resistor, MCR18-472EJ, metal, 4.7KΩ, 0.125W, 5%	ND0247EBD	094472225
R17	Resistor, MCR18-471EJ, metal, 470Ω, 0.125W, 5%	ND0169EBD	094471225
R18	Resistor, MCR18-824EJ, metal, 820KΩ, 0.125W, 5%	ND0440EBD	094824225
R19, 20	Resistor, MCR18-104EJ, metal, 100KΩ, 0.125W, 5%	ND0371EBD	094104225
R21, 22	Resistor, MCR18-103EJ, metal, 10KΩ, 0.125W, 5%	ND0281EBD	094103225
R23	Resistor, MCR18-272EJ, metal, 2.7KΩ, 0.125W, 5%	ND0224EBD	094272225
R24	Resistor, MCR18-222EJ, metal, 2.2KΩ, 0.125W, 5%	ND0216EBD	094222225
R25	Resistor, MCR18-272EJ, metal, 2.7KΩ, 0.125W, 5%	ND0224EBD	094272225
R26	Resistor, MCR18-472EJ, metal, 4.7KΩ, 0.125W, 5%	ND0247EBD	094472225
R27	Resistor, MCR18-273EJ, metal, 27KΩ, 0.125W, 5%	ND0316EBD	094273225
R28, 29	Resistor, MCR18-223EJ, metal, 22KΩ, 0.125W, 5%	ND0311EBD	094223225

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
R30-36	Resistor, MCR18-104EJ, metal, 100KΩ, 0.125W, 5%	ND0371EBD	094104225
R37, 38	Resistor, MCR18-103EJ, metal, 10KΩ, 0.125W, 5%	ND0281EBD	094103225
R39, 40	Resistor, MCR18-102EJ, metal, 1KΩ, 0.125W, 5%	ND0196EBD	094102225
R41	Resistor, MCR18-681EJ, metal, 680Ω, 0.125W, 5%	ND0183EBD	094681225
R42	Resistor, MCR18-152EJ, metal, 1.5KΩ, 0.125W, 5%	ND0206EBD	094152225
R43	Resistor, MCR18-472EJ, metal, 4.7KΩ, 0.125W, 5%	ND0247EBD	094472225
R44	Resistor, MCR18-104EJ, metal, 100KΩ, 0.125W, 5%	ND0371EBD	094104225
R45-50	Resistor, MCR18-221EJ, metal, 220Ω, 0.125W, 5%	ND0149EBD	094221225
R51, 52	Resistor, MCR18-104EJ, metal, 100KΩ, 0.125W, 5%	ND0371EBD	094104225
R53, 54	Resistor, MCR18-152EJ, metal, 1.5KΩ, 0.125W, 5%	ND0206EBD	094152225
R55-60	Resistor, MCR18-104EJ, metal, 100KΩ, 0.125W, 5%	ND0371EBD	094104225
R61	Not used		
R62	Resistor, MCR18-152EJ, metal, 1.5KΩ, 0.125W, 5%	ND0206EBD	094152225
R63-65	Resistor, MCR18-153EJ, metal, 15KΩ, 0.125W, 5%	ND0297EBD	094153225
	TRANSISTORS		
Q1, 2	Transistor 2SC2884Y, NPN	2SC2884Y	W00755001
Q3	Transistor 2SA1313Y, PNP	2SA1313Y	W00756001
Q4	Transistor μN2211, NPN	1TR0319	W00709000
Q5	Transistor 2SA1363, PNP	2SA1363	W00855001
Q6, 7	Transistor μN2112, PNP	1TR0325	W00757001
	MISCELLEANEOUS		
L1, 2	Coil, 560μH, ±10%, NL453232-561K	ACA9033	W00715000
L3	Coil, 470μH, ±10%, NL453232-471K	ACA9032	W00714000
FB1	Beads inductor, CB30322513		W00716000
X1	Oscillator, FAR-C4CB-08000000-MO2	ACA9034	W00758001
X2	Ceralock, CST2.457MG	ACA9035	W00759001

DC-DC CONVERTER WHOLE ASSEMBLY

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
8	DC-DC converter whole ass'y	XB1550	W00839001
9	PCB ass'y, Power		W00840001
#1	IC, MB3761, Voltage detector	MX6819	W00842001
C1	Capacitor, Ceramic, 0.1μF, +80%, −20%, 25V, DD306-249F104Z25		W00844001
C2	Capacitor, Electrolytic, 4.7μF, ±20%, 50V, UVS1H4R7MNA		Y44795601
C3	Capacitor, Electrolytic, 10μF, ±20%, 16V, UVS1C100MNA		Y41002601
C4	Capacitor, Ceramic, 0.1μF, +80%, −20%, 25V, DD306-249F104Z25		W00844001
C5, 6	Capacitor, Electrolytic, 100μF, ±20%, 16V, UVS1C101MNA		Y41012601
C7	Capacitor, Polyester, 22000pF, ±10%, 50V, QYX1H223KTP		Y52230110
C8	Capacitor, Polyester, 10000pF, ±10%, 50V, QYX1H102KTP		Y51020110
C9, 10	Capacitor, Electrolytic, 330μF, ±20%, 6.3V, UVS0J331MNA		Y43310601
D1, 2	Diode 1S2076		U04049000
D3	Shottky diode ERA82-004		U80580000
L1, 2	Coil, 100μH, ±10%, RCH875-101		W00846001
P1	Connector, 5267-02A		U15266000
P2	Not used		
P3	Jumper lead wire 9P		W00847001
Q1	Transistor, 2SA1115, PNP		132542001
Q2, 3, 4	Transistor, 2SC2603, NPN		132541001
Q5	Digital transistor RN1207, NPN		U41775000
Q6	Transistor, 2SC2603, NPN		132541001
Q7	Transistor, 2SC2655, NPN		W00843001
R1	Resistor, carbon, 22KΩ, 0.2W, 2%		090223710
R2	Resistor, carbon, 1.8KΩ, 0.2W, 2%		090182710
R3	Not used		
R4	Resistor, carbon, 10KΩ, 0.2W, 2%		090103710
R5	Resistor, carbon, 10KΩ, 0.2W, 5%		090103720
R6	Resistor, carbon, 2.2KΩ, 0.2W, 5%		090222720
R7	Resistor, carbon, 4.7KΩ, 0.2W, 5%		090472720
R8, 9	Resistor, carbon, 10KΩ, 0.2W, 5%		090103720
R10	Resistor, carbon, 1.8KΩ, 0.2W, 5%		090182720
R11	Resistor, carbon, 4.7KΩ, 0.2W, 5%		090472720

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
R12	Resistor, carbon, 100Ω, 0.2W, 5%		090101720
R13	Resistor, carbon, 10KΩ, 0.2W, 5%		090103720
R14	Resistor, carbon, 5.1KΩ, 0.2W, 5%		090512720
R15, 16	Resistor, carbon, 10KΩ, 0.2W, 5%		090103720
R17	Resistor, carbon, 22Ω, 0.2W, 5%		090220720
T1	Transformer, LC15		W00845001
ZD1	Zener diode HZ33		W00933000
ZD2	Zener diode HZ5ALL		U40161000
10	PCB ass'y, Panel	XB1576	W00852001
11	Power switch, slide		W00162001
12	LED (red) TLR208		W00163001
13	Resistor, carbon, 680Ω, 0.2W, 5%		090681720
14	Resistor, carbon, 100Ω, 0.2W, 5%		090101720
15	Jumper lead wire 5P		W00854001



NOTES:

A) RATED POWER OF UNSPECIFIED RESISTOR: 1/8W

B) #3: TC74HC00F, #7: TC74HC368F, #8: TC4584F

Fig. 12-1 Schematic Diagram of Main PCB

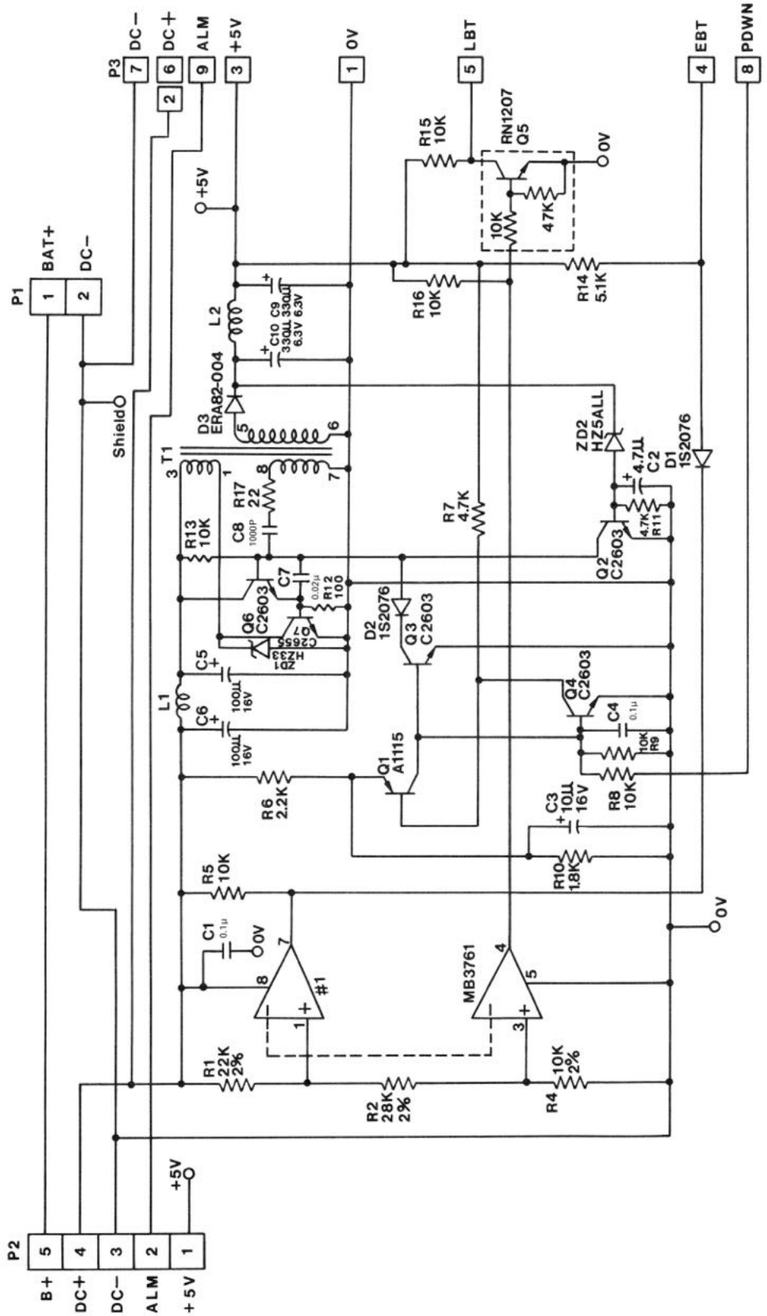


Fig. 12-2 Schematic Diagram of Power PCB

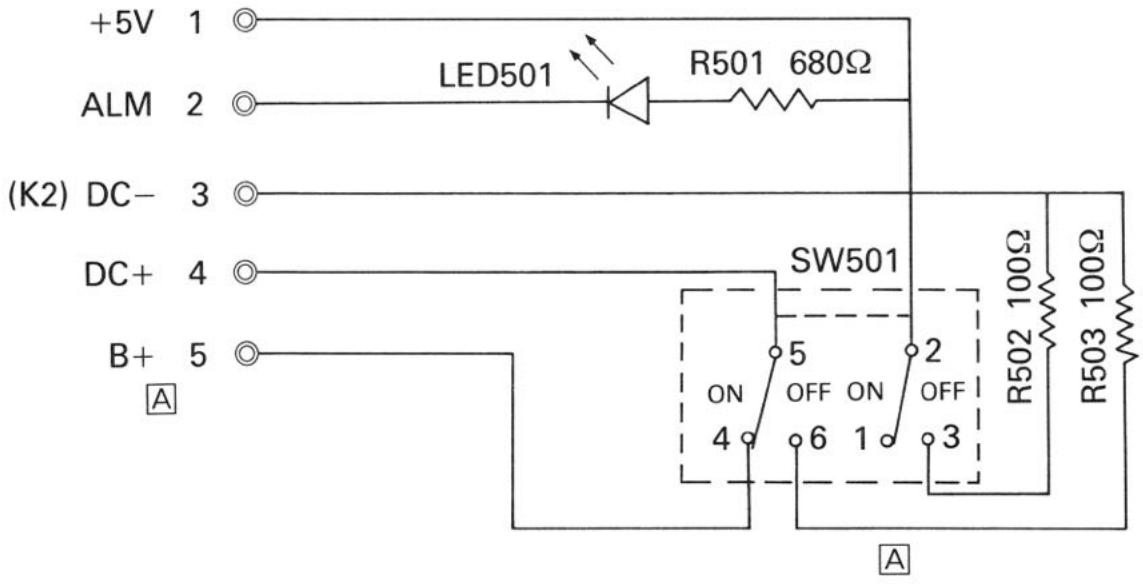


Fig. 12-3 Schematic Diagram of Panel PCB

12. SOFTWARE SECTION

12-1. Introduction of Software Section

Your Portable Disk Drive 2 can be used with any of the Tandy portable computers: the Model 100, the Tandy 102, or the Tandy 200.

This section describes the Portable Disk Drive 2's software, beginning with the format in which the drive stores data on the diskette.

Use this section hand-in-hand with the Portable Disk Drive 2 Operation Manual that comes with the drive.

12-2. Structure of Disk Data

This chapter describes the structure of data stored with a Portable Disk Drive 2. First, it looks at the physical divisions of the diskette. Then, it looks at the logical construction of a file.

12-2-1. Disk Sectors

At the factory, the Portable Disk Drive 2 diskettes are formatted to have 80 rings, or tracks, numbered 0-79. Each track is divided into two sectors, numbered 0 and 1. The sector is the smallest unit of a track that the disk drive can access (read from or write to) directly. In all, there are 160 sectors on a diskette (two sectors per track × 80 tracks per diskette), as shown in the following illustration:

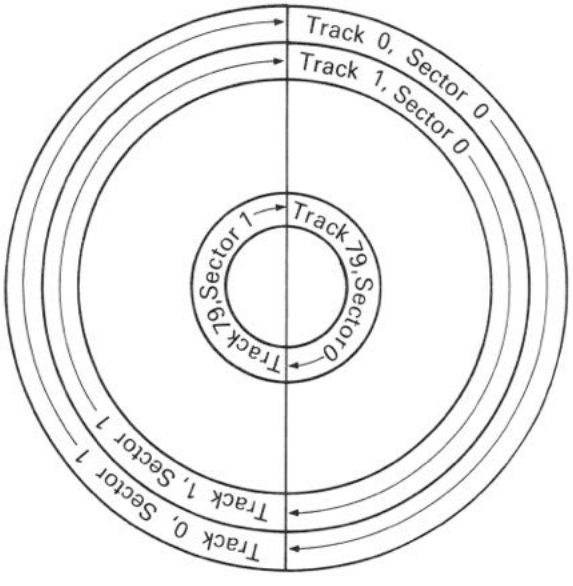


Fig. 12-1 Disk Sectors.

The sectors on Portable Disk Drive 2 diskettes are called hard sectors because they are permanent. They are established at the factory by an index hole on the spindle of the disk drive.

Locating Sectors

Whenever the computer needs to access data, it consults the disk directory to learn which sector the data is on. For example, the directory might indicate that the data is on Track 4, Sector 1. Given this information, the computer positions the disk drive head to the correct track (in this case, Track 4).

As the track spins beneath the drive head, the computer uses an index signal to recognize the appropriate sector when that sector comes along. For example, if the computer is looking for Sector 0 on the track illustrated in Fig. 12-2, the index signal looks for a 7.6 ms timing gap on the spinning diskette. When the drive head reads that gap, the computer knows it has found Sector 1.

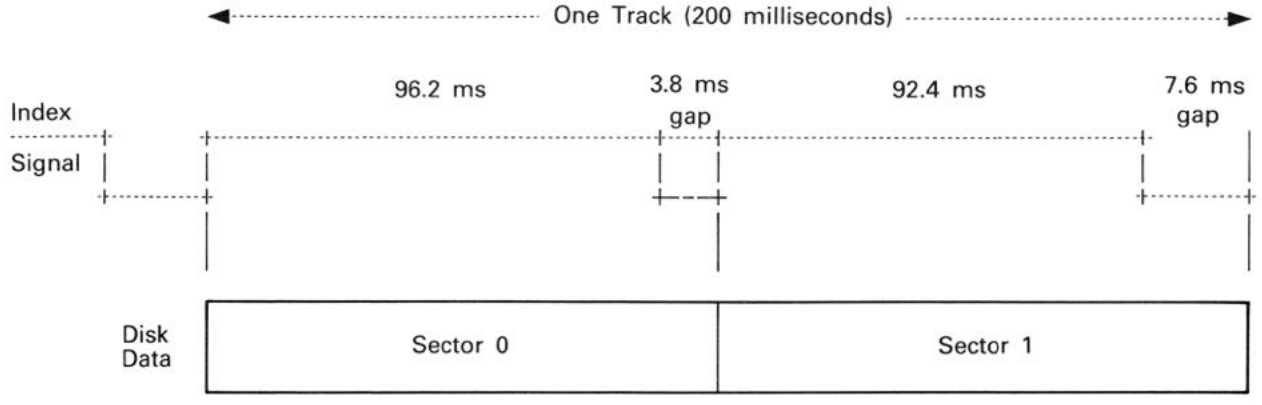


Fig. 12-2
The Relationship between the Index and the Hard Sector.

Note: The segments in Fig. 12-2 and in other illustrations in this manual are not drawn to scale. To get a clear understanding, always note the true measurements provided.

Parts of a Sector

A sector is divided into three parts: data, disk ID information, and disk control information. The control information consists of the preamble, startmark, and postscript. See Fig. 12-3 for the breakdown.

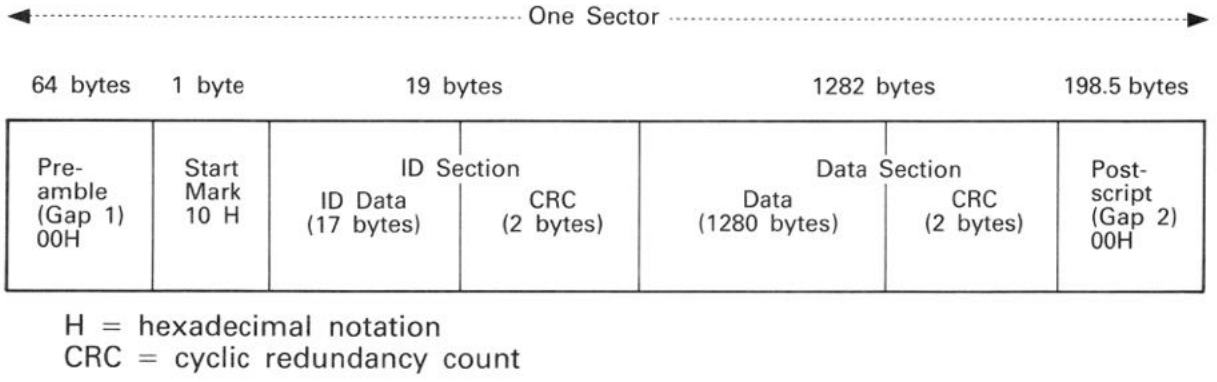


Fig. 12-3 A Sector.

Fig. 12-4 illustrates the format of the ID section of a sector.

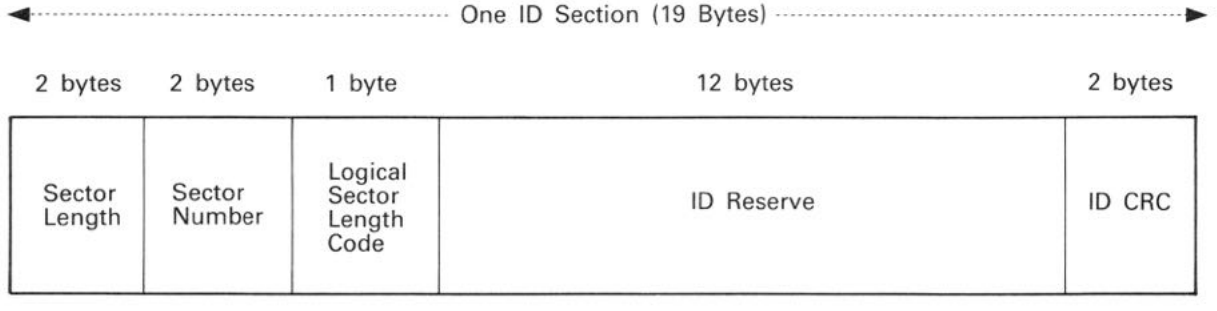


Fig. 12-4 The ID Section of a Sector.

12-2-2. Logical Construction of the Disk and Files

The first part of this section analyzes the various parts of the disk directory and how they pertain to a given file. The second part illustrates the structure of the file itself.

The Directory

The disk directory is located on Track 0, Sectors 0 and 1. It consists of 80 file control blocks (FCBs) and two space management tables (SMTs).

Each file is managed by its own FCB. The free sectors are managed by the SMT.

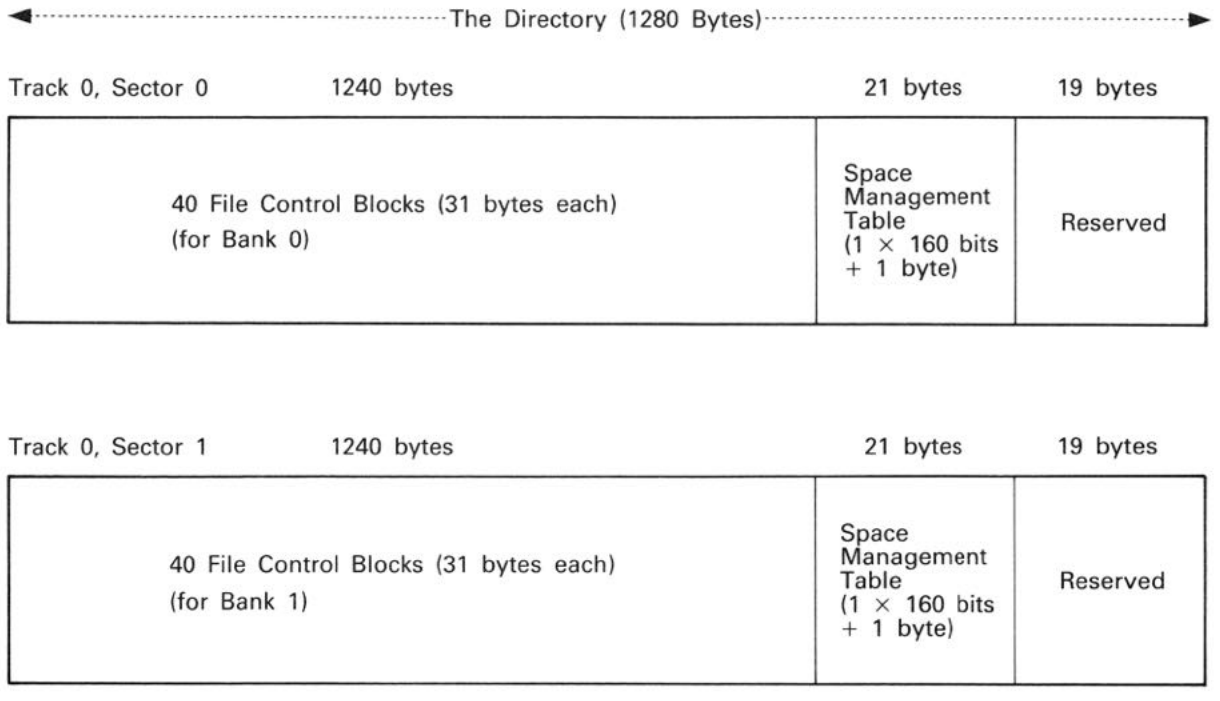


Fig. 12-5 The Disk Directory.

The File Control Blocks

One File Control Block consists of the following:

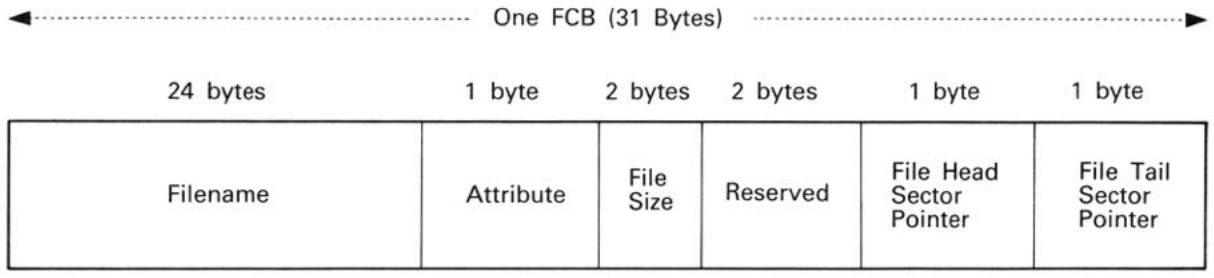


Fig. 12-6 An FCB.

Filename.

The filename is a text line consisting of a maximum of 24 characters. Fig. 12-7 illustrates the format of a filename.

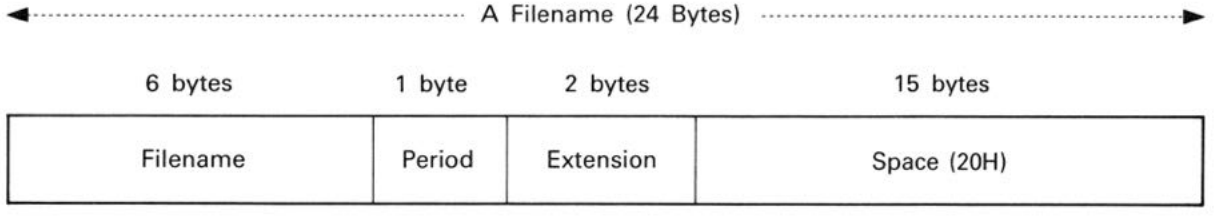


Fig. 12-7 Filename Format.

File Attribute.

Normally, when the system searches for a file, the designated file attribute has priority. However, when the Portable Disk Drive 2 is used with the Model 100, Tandy 102, or Tandy 200, the byte is always filled with the ASCII value of the character F, which instructs the system to ignore the file attribute.

File Size.

The file size takes up two bytes of the FCB. For a text file, the size is the length of the file, in bytes, minus the EOF byte. For a BASIC program, the size is the length of the pseudo code of the BASIC file.

Sector Pointers for File Head and Tail.

These pointers indicate the sectors at which the file begins and ends. Each pointer uses one byte of the FCB. The first seven bits are for the track number. The eighth bit is for the sector number.

The Space Management Table

In the SMT, one bit is assigned to each sector and is used for file management. The bit shows the status of the sector: 0 = not used, 1 = used.

In all, 20 bytes are used for file management (1 bit per sector × 160 sectors per disk = 160 bits, or 20 bytes).

The 21st byte of the SMT contains the used-sector counter, which keeps track of the number of used sectors.
One diskette has two of the same SMTs in Track 0, Sector 0 and Track 0, Sector 1.

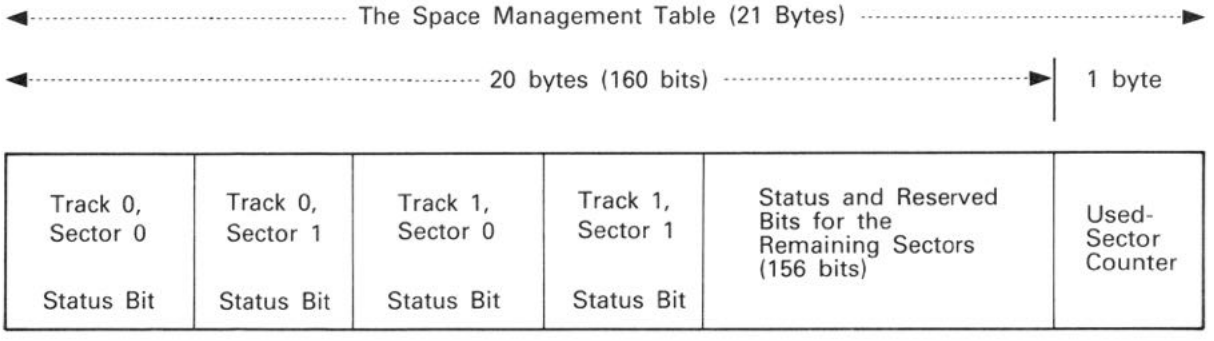


Fig. 12-8 The SMT.

Construction of a File

Here is a summary of the specifications for sequential files on a diskette in the Portable Disk Drive 2:

maximum length of file	=	65535 bytes
length of filename	=	24 bytes
maximum number of files	=	80 files
total disk capacity	=	202.24 kilobytes

The construction of a file is as follows:

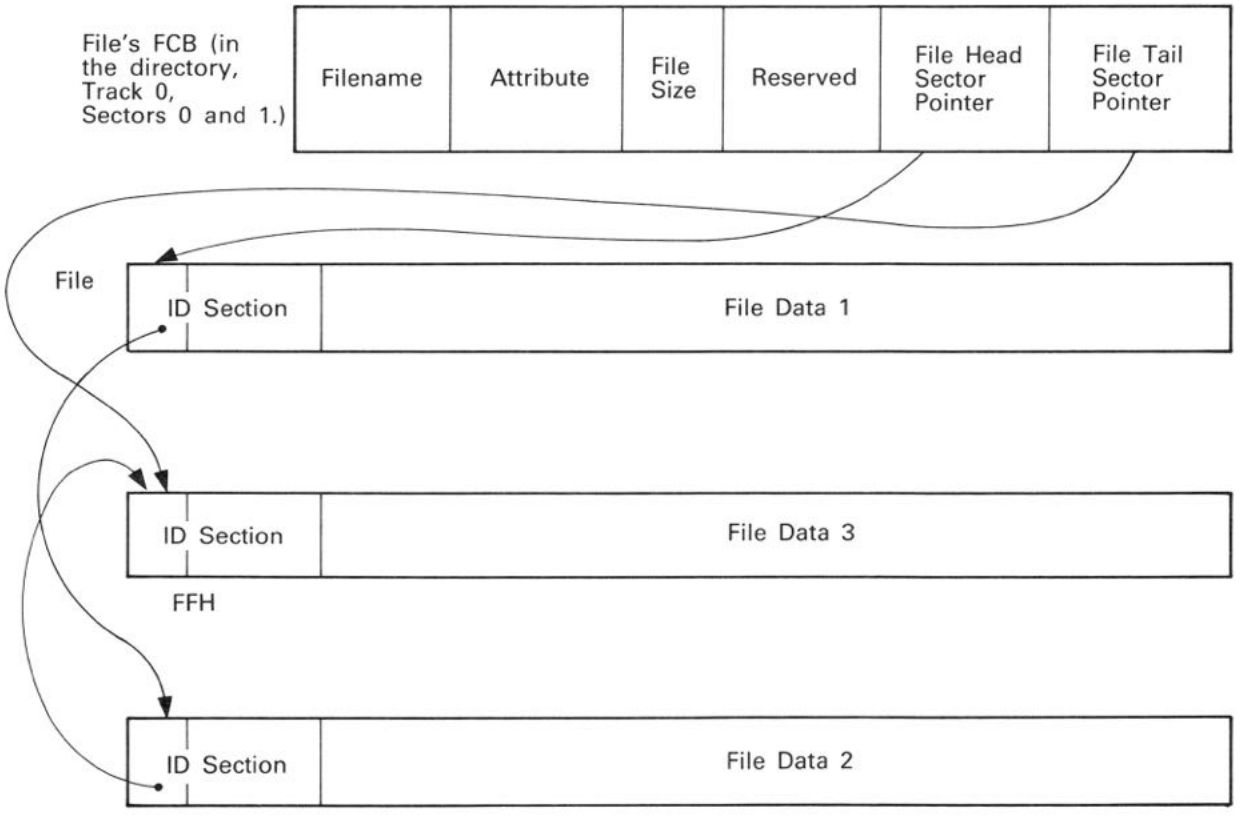


Fig. 12-9 Construction of a File.

12-3. Internal Software Operation

The key to the software operation of the Portable Disk Drive 2 is a device driver called FLOPPY. This driver is created during the IPL operation.

A device driver is any program that enables a computer to take advantage of a particular device, such as a printer or disk drive. In particular, FLOPPY is the file manager for the Portable Disk Drive 2. It provides the computer with the information that the computer requires for management of the drive's disk files.

12-3-1. Mode of Operation

The Portable Disk Drive 2 uses the Operation Mode, which is upwardly compatible with the Portable Disk Drive (Cat. No. 26-3808). The Initialization mode and the FDC-emulation mode in the Portable Disk Drive are not implemented in the Portable Disk Drive 2.

Operation mode is used to operate on the file data, the sector data, and the internal memory drive.

Note: See the Portable Disk Drive Operation Manual for more information on the commands available with the drive.

File Manager Installation

The following is a summary of what goes on "behind the scenes" during the IPL procedure:

1. You turn on the drive in the IPL condition.
2. The drive sends the first IPL code in BASIC to the computer.
3. The computer receives the code and executes it. It determines the model of the computer (Model 100, Tandy 102, or Tandy 200), and the computer sends the model type to the drive.
4. The drive receives the information, and loads the second IPL code for that model from the IPL disk. Then, it sends the second IPL code to the computer.
5. The computer loads the second program (sent in Step 4), and passes the control to that program.
6. Following the instructions from the program, the drive sends the main code of the file manager to the computer.
7. The second IPL code receives the main code of the file manager and creates the file FLOPPY.

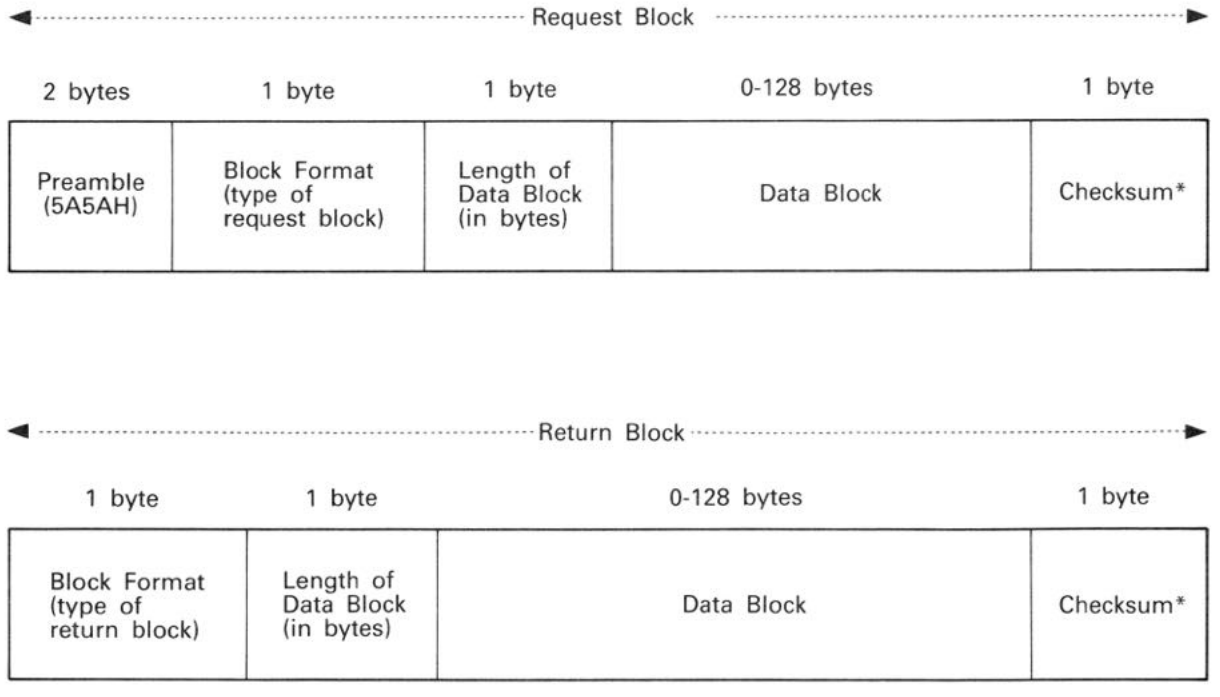
Block Communication

The computer controls the drive via block communication through the serial (RS-232C) interface. The computer sends a request block of data strings to the drive. In response, the drive sends a return block of data strings to the computer.

This exchange of information is termed a half-duplex block transfer because messages go in two directions, but in only one direction at a time. Drive control can be performed by either one transfer of blocks or by a combination of transfers. The determining factor is the type of instruction that the computer is giving.

Formats of the Communication Blocks

The formats of the request and return blocks are illustrated in Fig. 12-10. See "12-4. Communication Reference," for information on specific requests and responses.



* The checksum is the one's complement of the least significant byte of the number of bytes from the block format through the data block.

Fig. 12-10 Formats of the Communication Blocks.

12-4. Communication Reference

This chapter is a reference section to the various block transfers available with the Portable Disk Drive 2. It lists the communications alphabetically and according to their functions, as shown in this summary:

Function	Request Block Format	Return Block Format
Change Name of File	0DH *	12H
Check the Drive's Status	07H	12H
Close a File	02H *	12H
Create/Access a Directory Reference	00H *	11H or 12H
Delete a File	05H *	12H
Execute Program	34H	3BH
Format a Disk	06H	12H
Get the Data from the Drive's Memory	32H	39H
Get the Drive's Condition	0CH	15H
Get System Information	33H	3AH
Get Version Number	23H	14H
Open a File	01H *	12H
Read File Data	03H *	10H or 12H
Read/Write the Data in Sector Mode	30H	38H
Set the Data to Drive's Memory	31H	38H
Write File Data	04H *	12H

* You can modify the asterisked commands to use Bank 0 or 1. The other commands are not affected by the bank selector field.

About the Descriptions in this Chapter

Each function's description contains the complete format to use for the request block. If the request requires a message in return, the format of the response block is also shown.

Note: In the event of an error, the drive sends a response block in the 12H format. See "12-5-1. Error Codes".

The following abbreviations are used in the illustrations of the communication blocks:

P = Preamble (always contains the value 5A5AH)
Fmt = Block format
Len = Data block length
C = Checksum (defined in "12-3. Internal Software Operation")

Bank Selector

Several Operation mode commands, such as Open a File and Delete a File, can specify the disk bank to be affected. The disk bank that is treated by the command is described in the bank field bit of the block format. The contents of the block format byte are as follows:

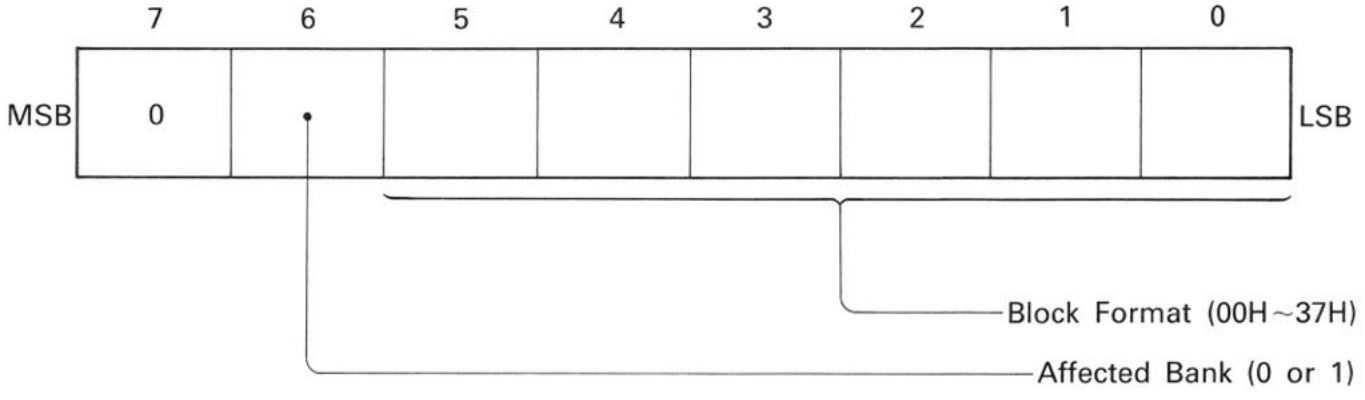


Fig. 12-11 Bank Field Bit.

The values for the block format and the data block length vary according to the particular communication. In each communication block, they are given in hexadecimal (H) format, in parentheses. Other items that are specific to a particular block are explained in the text.

Order of Block Transfers

The order in which you perform certain communication functions is critical. For example, you must create a reference about a file before you can open or delete that file. If you do not, a Sequence Error (3XH) occurs. See the sample sequences in "12-5-2. Flowcharts".

CHANGE NAME OF FILE

Changes the name of the file specified in a prior Create Directory Reference communication.

Note that the search form used in the prior Create/Access Directory Reference communication must be 00H. (See "Create/Access Directory Reference.")

REQUEST BLOCK

2 bytes	1 byte	1 byte	24 bytes	1 byte	1 byte
P (5A5AH)	Fmt (0DH)	Len (19H)	Filename	File Attribute	C

Request Block Items

filename — Specifies the new filename. It can be a maximum of 24 bytes long. You can use any alphanumeric characters in the filename, as long as you do not use the value 00H in the first byte.

file attribute — Specifies the new attribute of the file. Use any letter for attribute.

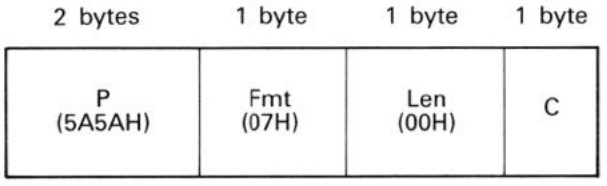
RETURN BLOCK

1 byte	1 byte	1 byte	1 byte
Fmt (12H)	Len (01H)	Error Code	C

CHECK THE DRIVE'S STATUS

Confirms that the disk drive is ready for use.

REQUEST BLOCK



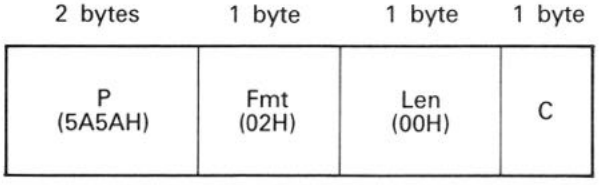
RETURN BLOCK

Refer to the 12H block (Change Name of File).

CLOSE A FILE

Closes the open file.

REQUEST BLOCK



RETURN BLOCK

Refer to the 12H block (Change Name of File).

CREATE/ACCESS DIRECTORY REFERENCE

Instructs the drive to create or access a directory reference about a file. You must create a reference before you can open or delete a file.

REQUEST BLOCK

2 bytes	1 byte	1 byte	24 bytes	1 byte	1 byte	1 byte
P (5A5AH)	Fmt (00H)	Len (1AH)	Filename	File Attribute	Search Form	C

Request Block Items

filename — Specifies the file for which you want the directory reference. The filename can be a maximum of 24 bytes long. You can use any alphanumeric characters in the filename, as long as you do not use the value 00H in the first byte.

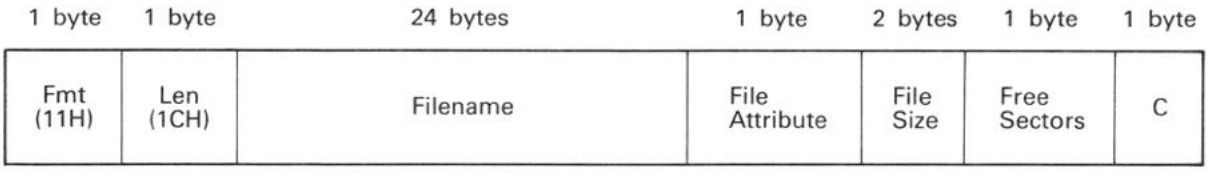
file attribute — Specifies the attribute of the file. The directory reference for the file with the given attribute is output before all others. Use any letter for the attribute.

search form — Specifies the form of the directory reference. Use any of the following:

- 00H to create a reference for a file to be opened or deleted.
- 01H to request the first directory information.
- 02H to request information for the next file.
- 03H to request information for the previous file.
- 04H to end the reference of the directory.

RETURN BLOCK

- If the operation is completed successfully:



Return Block Items

filename — The name of the file specified in the request. If you specified no file, the filename is filled with the value 00H. If you asked for directory information on the next file, and the reference past the end of the directory, the filename is also filled with the value 00H.

file attribute — Specifies the attribute of the file. If the filename is invalid (00H), the attribute also contains 00H.

file size — The size of the file. The preceding byte is significant. If the filename is invalid, the size is 0000H.

free sectors — The number of hard sectors available on the diskette. (One sector contains 1280 bytes.) The correct number returns even if the filename is invalid.

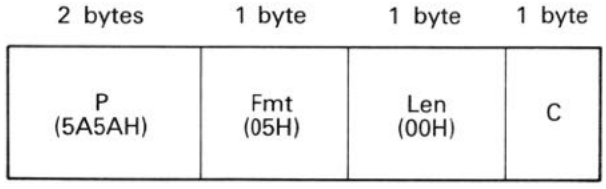
- If the operation is not completed successfully, refer to the 12H block (Change Name of File).

DELETE A FILE

Deletes the file specified in a prior Create Directory Reference communication.

Note that the search form used in the Create/Access Directory Reference communication must be 00H. (See "Create/Access Directory Reference.")

REQUEST BLOCK



RETURN BLOCK

Refer to the 12H block (Change Name of File).

EXECUTE PROGRAM

Puts the data in the CPU register and performs a subroutine call to the address designated.

REQUEST BLOCK

2 bytes	1 byte	1 byte	2 bytes	1 byte	2 bytes	1 byte
P (5A5AH)	Fmt (34H)	Len (05H)	Execute Address	A register value	X register value	C

Request Block Items

execute address — The address of the subroutine.

A register value — The data set in the A register before the subroutine call.

X register value — The data set in the X register before the subroutine call.

RETURN BLOCK

1 byte	1 byte	1 byte	2 bytes	1 byte
Fmt (3BH)	Len (03H)	A register value	X register value	C

Return Block Items

A register value — The A register value returned from the executed program.

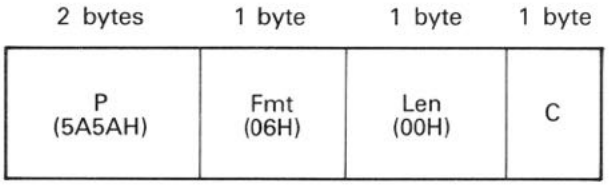
X register value — The X register value returned from the executed program.

Note: Set the execution program to the internal memory using a memory write. (See "Set the Data to the Drive's Memory".) In memory execution, the control is transferred to execution program.

FORMAT A DISK

Formats a disk and initializes the directory.

REQUEST BLOCK



RETURN BLOCK

Refer to the 12H block (Change Name of File).

GET THE DATA FROM THE DRIVE'S MEMORY

Gets the data from the memory built into the drive.

REQUEST BLOCK

2 bytes	1 byte	1 byte	1 byte	2 bytes	1 byte	1 byte
P (5A5AH)	Fmt (32H)	Len (04H)	Mode	Address	Request Data Byte	C

Request Block Items

mode — Specifies the object of the operation. Use either of the following:

- 00H to select the hard sector buffer. In this mode, the first byte of the data part of the hard sector corresponds to address 0000H, which you specify as address.
- 01H to select memory space. In this mode, the address you specify corresponds to the memory space address of the CPU built into the drive.

address — Specifies the address of the memory data requested. The preceding byte is significant.

request data byte — Requests the number of byte requested. The data with the number of byte ordered is returned from the address designated in address. The number of byte should be 1～125.

RETURN BLOCK

- If the operation is completed successfully:

1 byte	1 byte	1 byte	2 bytes	1-125 bytes	1 byte
Fmt (39H)	Len (4-80H)	Mode	Address	Memory Data	C

Return Block Items

len	Block data length.
mode	This is the same mode as for a memory write (31H).
address	This is the same address as for a memory write (31H).
memory data	The data that is returned from the memory.

- If the operation is not completed successfully:

1 byte	1 byte	1 byte	1 byte
Fmt (38H)	Len (01H)	Error Code	C

Return Block Items

error code	Refer to "12-5-1. Error Code".

GET THE DRIVE'S CONDITION

Requests information about the drive's condition.

REQUEST BLOCK

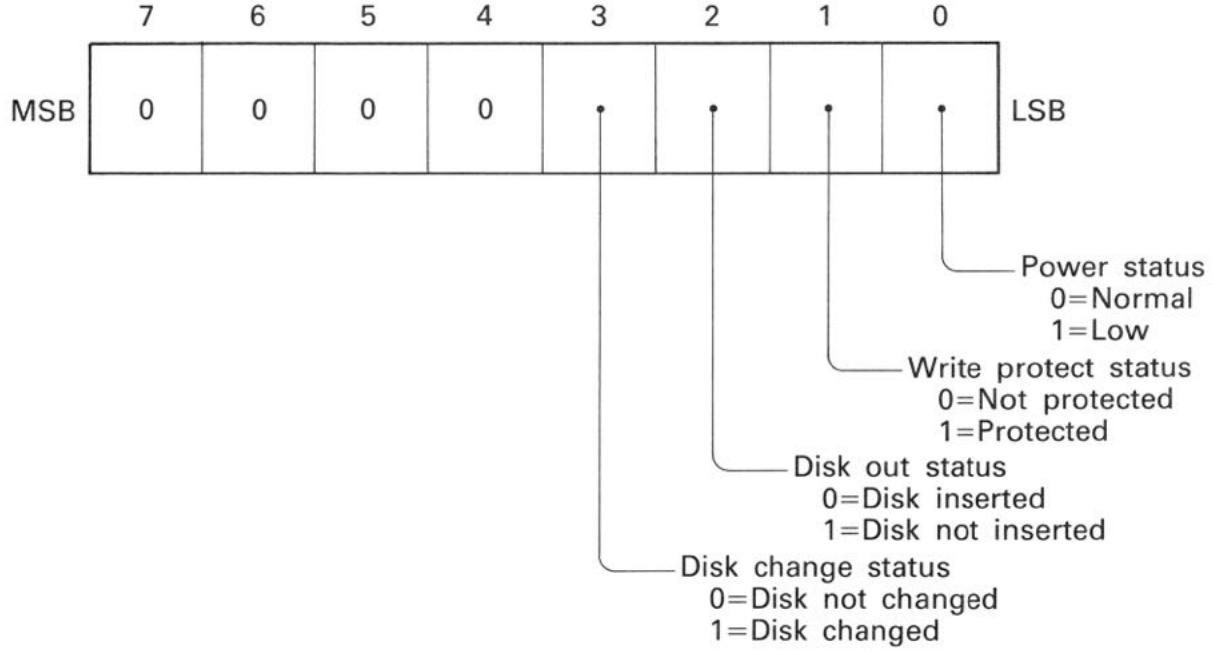
2 bytes	1 byte	1 byte	1 byte
P (5A5AH)	Fmt (0CH)	Len (00H)	C

RETURN BLOCK

1 byte	1 byte	1 byte	1 byte
Fmt (15H)	Len (01H)	Device Condition	C

Return Block Items

device condition — Each bit is assigned as follows:

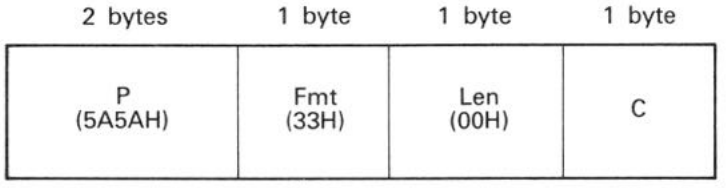


Note: • If the diskette is not inserted, the write protect bit is always 1.
• After execution of this command, the condition is not changed.

GET SYSTEM INFORMATION

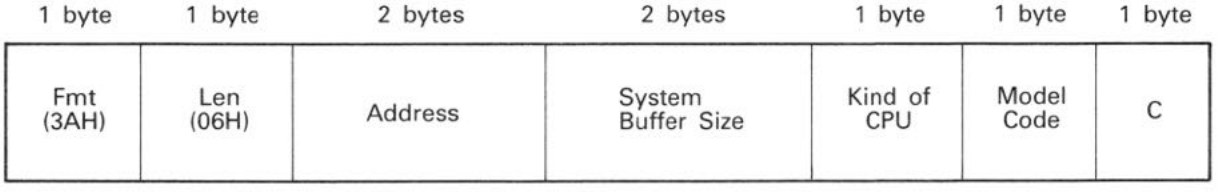
Requests system information.

REQUEST BLOCK



2 bytes	1 byte	1 byte	1 byte
P (5A5AH)	Fmt (33H)	Len (00H)	C

RETURN BLOCK



1 byte	1 byte	2 bytes	2 bytes	1 byte	1 byte	1 byte
Fmt (3AH)	Len (06H)	Address	System Buffer Size	Kind of CPU	Model Code	C

Return Block Items

address — The first byte address of hard sector data part. It is 8013H.

system buffer size — Buffer size of hard sector data part. It is 0500H.

kind of CPU — Classification of the CPU built in the drive. It is 10H (HD6301).

model code — E1H (the model code that returned by system version information).

GET VERSION NUMBER

Requests system version information.

REQUEST BLOCK

2 bytes	1 byte	1 byte	1 byte
P (5A5AH)	Fmt (23H)	Len (00H)	C

RETURN BLOCK

1 byte	1 byte	2 bytes	1 byte	2 bytes	2 bytes	1 byte	2 bytes	1 byte	1 byte	3 bytes	1 byte
Fmt (14H)	Len (0FH)	①	②	③	④	⑤	⑥	⑦	⑧	⑨	C

Return Block Items

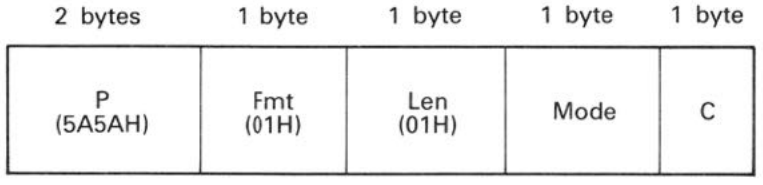
① system version number	It is 4110H in this system
② number of sides	It is 01H
③ number of tracks	It is 0050H
④ sector length	It is 0500H
⑤ number of sectors per track	It is 02H
⑥ number of directory entries	It is 0028H
⑦ maximum channel number	It is 00H (the number of files that can be open at the same time-1)
⑧ model code	It is E1H
⑨ spare bytes	It is 00H

OPEN A FILE

Opens the file specified in a prior Create Directory Reference communication. You can open only one file at a time.

Note that the search form used in the Create/Access Directory Reference communication must be 00H. (See "Create/Access Directory Reference.")

REQUEST BLOCK



Request Block Items

mode — Specifies the mode in which you want the file to be opened. Use any of the following:

01H	to open the file (new) in write mode.
02H	to open the file (existing) in append/write mode.
03H	to open the file (existing) in read mode.

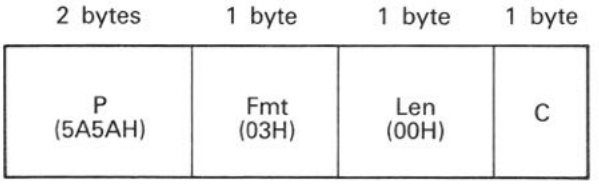
RETURN BLOCK

Refer to the 12H block (Change Name of File).

READ FILE DATA

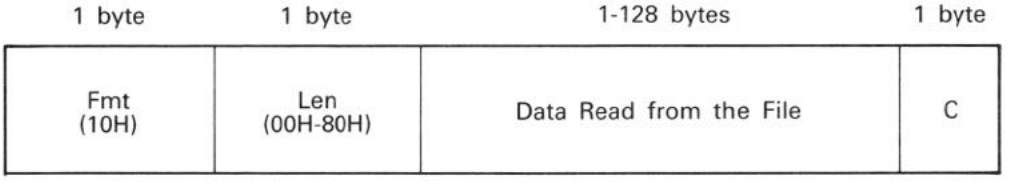
Reads the data in the open file.

REQUEST BLOCK



RETURN BLOCK

- If the operation is completed successfully:



Return Block Items

len — Specifies the number of bytes of data read from the file. If the amount of data remaining is more than 128 bytes, the data block length (len) is 128 bytes. If the amount is equal to or less than 128 bytes, len is the same as the amount.

- If the operation is not completed successfully, refer to the 12H block (Change Name of File).

READ/WRITE THE DATA IN SECTOR MODE

Loads the disk data, by hard sector units, to the buffer built into the drive, or writes the contents of the buffer.

REQUEST BLOCK

2 bytes	1 byte	1 byte	1 byte	2 bytes	1 byte	1 byte	1 byte
P (5A5AH)	Fmt (30H)	Len (05H)	Mode	Track Number	Side Number	Sector Number	C

Request Block Items

mode — Specifies the operation you want to perform. Use any of the following:

- 00H to load the specified hard sector into the buffer.
- 01H to write the contents of the buffer to the specified hard sector.
- 02H to write the contents of the buffer to the specified hard sector and then verify the write.

track number — Specifies the track (0000-04FH).

side number — Specifies the side (00H).

sector number — Specifies the sector (00H or 01H).

RETURN BLOCK

Refer to the 38H block (Get the Data from the Drive's Memory).

SET THE DATA TO DRIVE'S MEMORY

Sets the data to the memory built into the drive.

REQUEST BLOCK

2 bytes	1 byte	1 byte	1 byte	2 bytes	1-125 bytes	1 byte
P (5A5AH)	Fmt (31H)	Len (4-80H)	Mode	Address	Write Data	C

Request Block Items

mode — Specifies the object of the operation. Specify either of the following:

- 00H — to select the hard sector buffer. In this mode, the first byte of the data part of the hard sector corresponds to address 0000H, which you specify as address.
- 01H — to select memory space. In this mode, the address you specify corresponds to the memory space address of the CPU built into the drive.

address — Specifies the address you want the data to go to. The preceding byte is significant.

write data — The data that you are setting in memory.

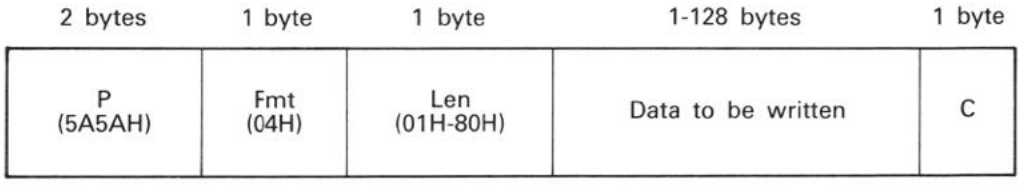
RETURN BLOCK

Refer to the 38H block (Get the Data from the Drive's Memory).

WRITE FILE DATA

Writes data to the open file.

REQUEST BLOCK



Request Block Items

len — Specifies the number of bytes in the data to be written.

In the event of an error, the system returns an error code. Otherwise, no block is returned.

RETURN BLOCK

Refer to the 12H block (Change Name of File).

12-5. Appendices

12-5-1. Error Codes

If an error occurs while the Portable Disk Drive 2 is in operation mode, the drive sends an error code in one of the following formats:

1 byte	1 byte	1 byte	1 byte
Fmt (12H)	Len (01H)	Error Code	C

1 byte	1 byte	1 byte	1 byte
Fmt (38H)	Len (01H)	Error Code	C

The details of the error codes are as follows:

Category	Code	Content	Related request block Block form														
			00H	01H	02H	03H	04H	05H	06H	07H	0CH	0DH	23H	30H	31H	32H	33H	34H
Normal	00H	Normal return		○	○		○	○	○	○		○		○	○			
File	10H	Designated file doesn't exist		○				○				○						
	11H	Designated file exists		○								○						
Sequence	30H	Filename is not designated		○														
	31H	Directory search doesn't start		○														
	35H	Bank designation error	○	○		○	○	○										
	36H	Parameter error	○	○			○							○	○	○		
	37H	Open format mismatch				○												
	3FH	End of file				○												
Disk I/O	40H	No start mark	○	○	○	○	○	○	○			○		○				
	41H	CRC check error of ID part	○	○	○	○	○	○				○		○				

Category	Code	Content	Related request block Block form																
			00H	01H	02H	03H	04H	05H	06H	07H	0CH	0DH	23H	30H	31H	32H	33H	34H
Disk I/O	42H	Hard sector length error	○	○	○	○	○	○				○		○				
	44H	Format verify error							○									
	46H	Format interruption							○									
	47H	Erase offset error			○		○	○				○		○				
	49H	CRC check error of data part	○	○	○	○	○	○				○		○				
	4AH	Hard sector no. error	○	○	○	○	○	○				○		○				
	4BH	Read data timeout	○	○	○	○	○	○	○			○		○				
	4DH	Hard sector no. error	○	○	○	○	○	○				○		○				
Protect	50H	Disk write protected			○		○	○	○			○		○				
	5EH	SMT un-initialized diskette	○															
	5FH	Write protect to 26-3808 diskette		○				○				○		○				
File territory	60H	Directory entry full		○								○						
	61H	Disk territory full					○											
	6EH	File too long					○											
Condition of diskette	70H	Diskette not inserted	○	○	○	○	○	○	○	○		○		○				
	71H	Diskette change error	○	○	○	○	○	○				○						
Sensor	80H	No index signal	○	○	○	○	○	○	○			○		○				
	81H	Abnormal Track 0 signal	○	○	○	○	○	○	○			○		○				
	82H	Abnormal index signal	○	○	○	○	○	○	○			○		○				
Communi-cation*	(D0H)	Overrun Framing error	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	(D1H)	Block checksum error																
	(D2H)	Receive buffer overflow																
	(E0H)	String interval timeout																

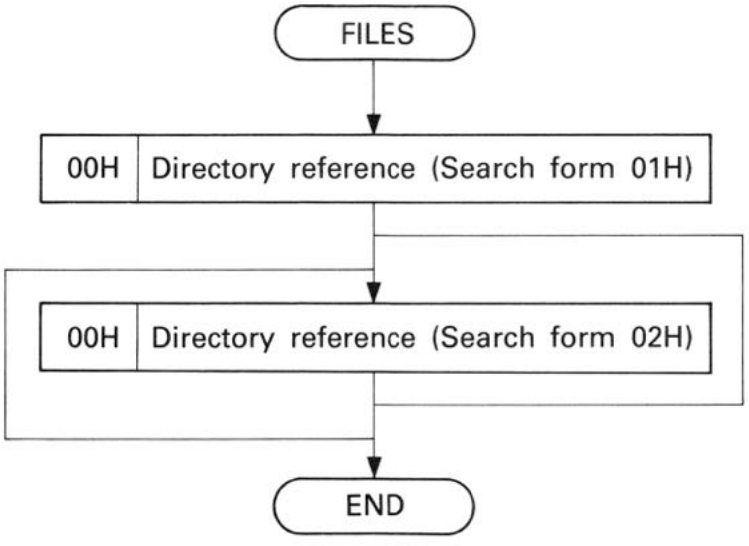
* The codes for communication errors are not returned. They are only for internal use by the drive.

12-5-2. Flowcharts

The following flowcharts illustrate some basic file operations you might perform. Use them as a guide to the order in which to send communications to the drive.

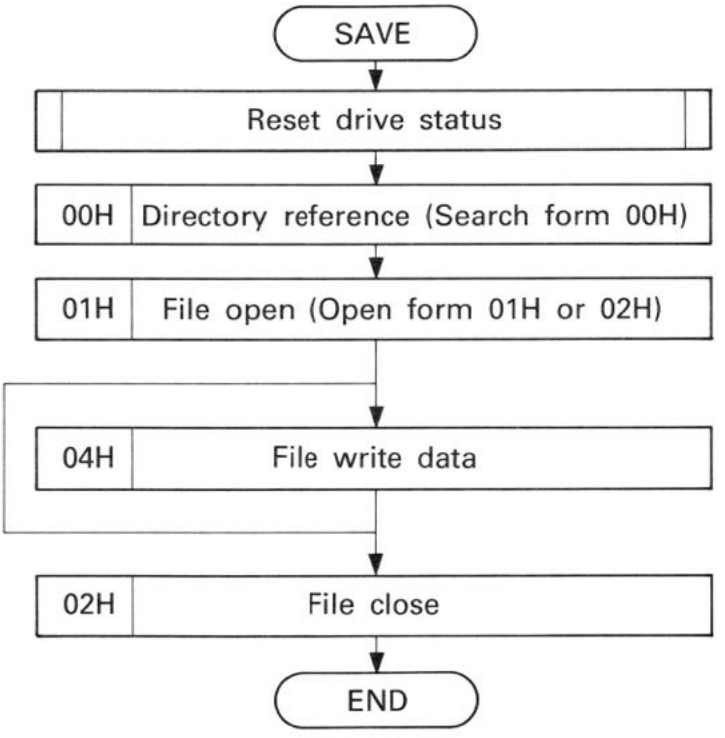
If any error other than a communication error occurs in the middle of a sequence, you need to start the sequence again.

Create/Access a Directory Reference



1. Start a directory reference.
2. Refer to the next directory.

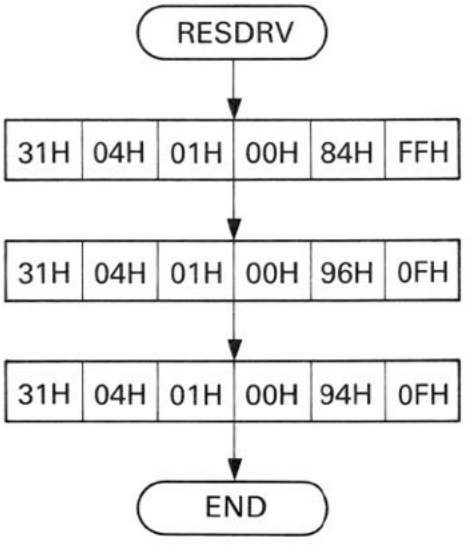
Write Data To a File



Refer to "Reset Drive Status".

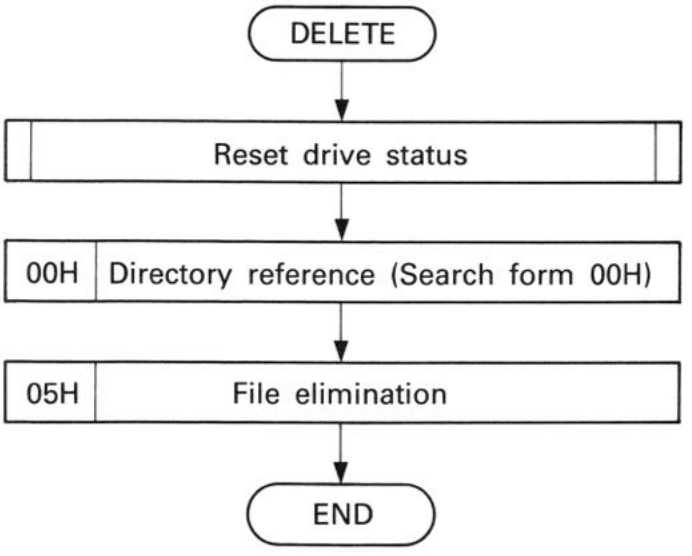
1. Specify the file to open.
2. Open the file in write mode
3. Send the data to be saved.
4. Close the file.

Reset Drive Status



1. Set FFH to memory address 0084H.
2. Set 0FH to memory address 0096H.
3. Set 0FH to memory address 0094H.

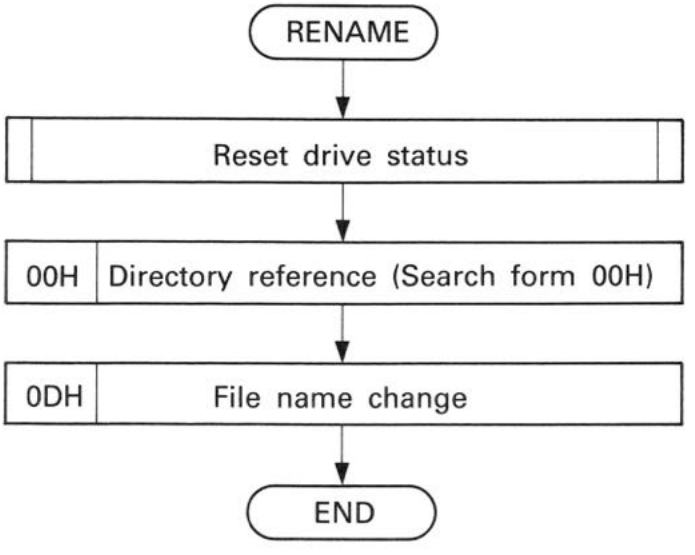
Delete a File



1. Specify the file to read.

2. Delete the file.

Rename a File



Refer to "Reset Drive Status".

1. Specify the file to rename.

2. Rename the file.

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