THE STARLET TECHNICAL NOTEBOOK FOR THE PC-8401A

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NOTICE

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CHAPTER 1

Specification of the MENU in the PC-8401A

DUPLICATE FILE NAMES IN ROM AND RAM-DISK OR DISK

When choosing a file name for a program to be saved on disk, either the RAM-disk or the micro floppy disk, it is necessary to follow this rule: Avoid using, and therefore duplicating, a name already used by the ROM's application programs, or by the Menu's CP/M programs, i.e. WS.COM, or PIP.COM, etc.

If this rule is not followed, the saved filename will be indistinguishable from the ROM filenames by the PC-8401A. When the filename is invoked, the ROM program or the Menu program will be executed instead of the saved program.

The execution searchpath begins with the ROM and Menu programs and, if the filename is not found, the search then proceeds to the saved programs. Duplicate filenames could exist, however, no duplicate will be noted as far as the computer is concerned. This is because once the specified filename is found in the ROM's or Menu program's directory listings, further searching is terminated, the file is simply loaded and executed.

There are only two ways to recover the use of a duplicated filename. One way is to place a drive descriptor in front of the name, eg. A:filename. This works for any duplicated ROM application program names, and informs the processor to load and execute the saved file from the specified device. However, this way will not work for duplicate Menu program names.

The other way, which will work in all cases, is to change the duplicate filename to a unique name by using the RENAME function. This always works because it removes the duplication of names.

BAD DIRECTORY

When a directory listing appears with "garbage" characters registered as filenames, the directory contents, and associated files may be unrecoverable. The Bad Directory could have one or more of the following causes:

1. Failure to format RAM #1 after the initial power on, or failure to format the RAM Cartridge (RAM #2) after Option Mode is selected to switch to the 64K CP/M mode.
2. Low battery in RAM Cartridge.
3. Bad directory on disk.

RAM #1 (internal to PC-8401A) must be formatted immediately after you power up the PC-8401A for the very first time (this being the 32K mode.) RAM #2 (external to the PC-8401A, in the RAM Cartridge) must be formatted immediately after Option Mode is used to switch to the 64K CP/M mode. This must also be done if the RAM Cartridge is being used in the 32K mode as the B: RAM-disk drive.

Another cause of "garbage" is erroneous machine language programs. They may inadvertantly destroy the directory area of the RAM-disk. In this event, the phrase "Bad directory" may appear on the screen and RAM #1 will have to be reformatted.

When a new RAM Cartridge is to be used, the protective battery seal must be removed before its insertion into the PC-8401A. If this is not done, when the power is removed from the machine, the RAM Cartridge will have no backup power to continue retaining any information. It is a good idea to keep track of the usage time on the special battery in the RAM Cartridge. Replace it, whether it needs it or not, every six months.

The first time a micro floppy diskette is used in the floppy disk system, you must format it. Formatting writes a new magnetic structure for data storage on the disk.

If a condition that causes garbage on the screen also causes the computer to operate erratically or unusually, a Cold Boot can be performed by depressing the reset button at the rear of the computer. It is advisable at that point, if the RAM-Disk is in use, to reformat it. The micro floppy need not be reformatted.

DEVICE NAMES

Since the PC-8401A can support an internal RAM-disk, an external RAM-disk Cartridge, external micro floppy disk drives, and two different memory modes of operation (32K and 64K,) the device names used to address the RAM-disk and micro floppy disks will vary according to the peripherals attached, and the current memory mode selected. The following table illustrates the device names used for the various combinations:

32K CP/M Mode

Without peripherals	Internal RAM-disk is A:
With RAM cartridge	Internal RAM-disk is A: RAM-disk cartridge is B:
With Floppy Disk	Internal RAM-disk is A: Mirco Floppy Drive #1 is B: Micro Floppy Drive #2 is C:
With Cassette	1200 Baud Cassette is CAS: 1200 Baud Cassette is CAS1: 600 Baud Cassette is CAS2:

(See Note below)

64K CP/M Mode

With RAM cartridge	RAM-disk cartridge is A:
With Floppy Disk	Micro Floppy Drive #1 is A: Micro Floppy Drive #2 is B:
With Cassette	1200 Baud Cassette is CAS: 1200 Baud Cassette is CAS1: 600 Baud Cassette is CAS2:

NOTE: The default for CAS: (no number specified) is CAS1:. The 600 Baud format is identical to the PC-8201A .DO file format.

WARM START AND COLD START

Due to this special implementation, the PC-8401A computer thinks that it's CP/M is always running, even through a power off and subsequent power on. That is because, as part of the power-off sequence, the PC-8401A saves all current operating data, including all internal registers, the program counter and stack. All the values in memory are retained by the CMOS memory circuitry, with trickle power from the batteries. The computer, upon powering back up, simply restores what it had saved when power was removed, and resumes what it was doing. This resumption is very different from a typical CP/M implementation because, in the typical CP/M computer, a power-on forces a complete Cold Start.

If a bug or erroneous situation occuring in a program causes the PC-8401A to hang (ignore any requests from the keyboard, due to an endless loop condition), a Cold Start may be forced. To reset CP/M to a known operational state perform any of the following:

- Press the Reset Button
- Press Shift & Stop during Power-on
- Change Device Configuration during power off.

Upon performing a Cold Start with any of the above, the PC-8401A is set to the 32K CP/M mode with the LCD as the console display device. The system Date & Time should be manually reset to current values, because they are lost by performing this process.

A NOTE ABOUT THE UPDATED TIME DISPLAY

The current Date & Time appears on the top of the Menu screen and is updated once every second. However, when the Menu is performing a task (reading the disk or running a program for instance) the time will not be updated. Upon completion of the task, the Menu will resume the constant update of the display with no loss of time, i.e. the clock will remain accurate despite the I/O request.

CHAPTER 2

The PC-8401A CP/M Environment

SECTION 1

OVERVIEW

This document has been prepared to summarize the environment of the PC-8401A CP/M system, which includes the memory map, the contents of Page Zero, and the method of BIOS and BDOS calls.

From the application programmer's point of view, the PC-8401A has 3 modes:

1. 32K CP/M mode
2. 64K CP/M mode
3. ROM program mode

The first two modes are standard CP/M environments, and require no special procedures to adapt standard CP/M application programs.

The third mode, the ROM program mode, works in a special environment. Programmers need to know the details of the memory mode and system locations, the contents of Page Zero, and the special ROM directory structure in order to register their ROM program name into the main menu.

SECTION 2

32K CP/M MODE

MEMORY MAP

Address	Contents	Size
0FFFFH		
	BIOS	2.5Kbytes
0F600H		
	BDOS	3.5Kbytes
0E800H		
	Open	32Kbytes
06800H		
	TPA	26Kbytes
00100H		
	Page Zero	
00000H		

The size of the TPA area is 26 Kbytes. This is the same TPA size of a 31K CP/M system when the CCP area is overwritten.

There is one thing programmers need to keep in mind about this mode. As shown in the memory map above, the BDOS always begins at 0E800H in this mode. Some CP/M application programs assume that the BDOS is located immediately above the very end of the TPA.

The PC-8401A resolves this problem by faking a BDOS entry point immediately above the TPA end. This is discussed in a later section. (The RAM addressed from 06800H to 0E800H is used as the drive A: RAM disk.)

PAGE ZERO

The Page Zero configuration is compatible with the standard CP/M Page Zero as shown below:

LOCATION	CONTENTS
00000H - 00002H	A jump to the warm start entry in the BIOS
00003H - 00003H	IO byte.
00004H - 00004H	Current default drive number
00005H - 00007H	A jump to the BDOS entry. A word at address 00006H is the lowest address in memory used by the BDOS.
00008H - 0000FH	RST 1 location. Internally used by the BIOS
00010H - 00017H	RST 2 location. A jump to the extended BIOS entry.
00018H - 0002FH	RST 3 through RST 5. Internally used by the BIOS and hardware.
00030H - 00037H	RST 6 location. Not used, but reserved by CP/M.
00038H - 0003FH	RST 7 location. Not used, but reserved by CP/M.
00040H - 0004FH	Not used.
00050H - 0005BH	Not used, but reserved by CP/M.
0005CH - 0007CH	Default FCB created by the CCP.
0007DH - 0007FH	Optional default random record position.
00080H - 000FFH	Default DMA address

BIOS CALLS

The 17 defined CP/M BIOS routines can be used exactly the same way as in the standard CP/M convention. The BIOS jump vectors are located at address 0F600H through 0F632H. Although the addresses are fixed, an application program can use the address field of the jump at address 00000H (the jump to the Warm Start entry point) to compute the page address of the vector table.

An extended BIOS call is made by issuing the RST 2 instruction with the extended BIOS call function number in the C register. (Refer to the extended BIOS specifications for details on the extended BIOS functions and their usage.)

FAKED BDOS ENTRY

As shown in the memory map, the TPA and BDOS are not contiguous in this mode. Some CP/M application programs find CP/M's TPA area by referencing the address field of the jump to the BDOS at address 00005H. If a jump to the actual BDOS entry at 0E806H is placed there, those application programs would fail to correctly determine the highest TPA address they can use. To resolve this problem, when in the 32K mode, address 00005H holds a jump to a faked BDOS entry at 06806H rather than the real BDOS entry at 0E806H.

Although not mentioned in the memory map, the hardware duplicates the BDOS code from 0E800H through 0FFFFH into addresses 06800H through 07FFFH. Address 00005H holds a jump to the duplicated BDOS entry point (06806H) rather than the real one. Therefore, this gives the ACTUAL highest TPA address that can be used by those application programs which reference 00005H to determine CP/M's TPA size.

Please note that the hardware does a simple duplication and the duplicated code is not necessarily executable. This is due to the fact that the address fields are not updated. The destination of the first jump in the duplicated BDOS (at address 06806H) is a jump instruction into the real BDOS. Therefore, any BDOS calls reach the real BDOS instantly, and cause no problem.

SECTION 3

64K CP/M MODE

MEMORY MAP

Address	Contents	Size
0FFFFH		
	BIOS	2.5Kbytes
0F600H		
	BDOS	3.5Kbytes
0E800H		
	TPA	58Kbytes
00100H		
	Page Zero	
00000H		

The size of the TPA area is 58 Kbytes. This is the same TPA size of a 63K CP/M, when the CCP area is overwritten.

PAGE ZERO

The Page Zero configuration is compatible with the standard CP/M Page Zero, as shown in the description of the 32K CP/M mode. Refer to it for further details of the Page Zero contents.

BIOS CALLS

BIOS calls are made in the same manner as in the 32K CP/M mode. They are completely compatible with the standard CP/M convention.

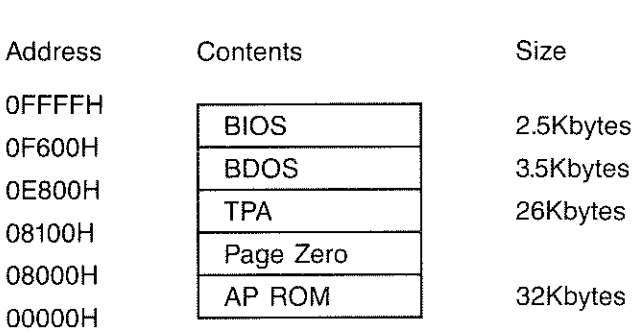
NO FAKES

Unlike the 32K mode, the 64K mode does not require a faked BDOS entry table. The TPA and BDOS are contiguous. This mode is completely standard, except for a few minor patches that have been made in the BDOS. Refer to the DOS patch specifications for further details about the patches.

SECTION 4

ROM PROGRAM MODE

MEMORY MAP



ROM programs run in this mode. The selected ROM is located at the lower half of the CPU addressing space. 26K of RAM is provided for data storage and bookkeeping purposes for the ROM application programs.

PAGE ZERO

In this mode, the CP/M Page Zero is located at addresses 08000H through 080FFH as shown below:

LOCATION	CONTENTS
08000H - 08002H	A jump to the warm start entry in the BIOS.
08003H - 08003H	IO byte.
08004H - 08004H	Current default drive number
08005H - 08007H	A jump to the BDOS entry. A word at address 00006H is the lowest address in memory used by the BDOS.
08008H - 0804FH	Not used.
08050H - 0805BH	Not used, but reserved by CP/M.
0805CH - 0807CH	Default FCB created by the CCP.
0807DH - 0807FH	Optional default random record position.
08080H - 080FFH	Default DMA address

Although a jump to the BDOS entry is placed at 08005H, the application program can use the standard CALL 00005H as well.

To return to CP/M, jump to 08000H instead of 00000H. The jump at address 00000H, in the ROM program mode, is not a jump to the Warm Start entry, but to the system initialization code.

BIOS CALLS

BIOS calls are made in the same manner as in the 32K CP/M mode. They are completely compatible with the standard CP/M convention.

SPECIAL CONSIDERATIONS

Some special things to consider when in the ROM Program Mode are listed below:

1. The code and data segments must be separated. The TPA is used for the data area. The program code itself is stored and executed from ROM. The code must be free of errors.

2. The TPA begins at address 08100H instead of 00100H.

3. Page Zero is located at address 08000H through 08100H as has been explained.

4. The start address and name of the program, which is to appear in the MENU, are stored at fixed locations in the ROM. Refer to the ROM specifications for more detailed information.

With few exceptions, as noted above, application programs can use the BDOS and BIOS functions as in a normal CP/M environment.

CHAPTER 3

Notes for Use of XSUB Under the PC-8401A CP/M

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There are few restrictions to the use of XSUB.

1. XSUB cannot be used in the 32K CP/M mode.

2. XSUB cannot be used with a ROM program in either the 32K or the 64K CP/M mode.

   When a ROM program is invoked by SUBMIT, XSUB is automatically terminated. SUBMIT is still active.

3. If a BDOS error occurs during operation of a CCP command (pip, dir, etc), XSUB is terminated. SUBMIT is still active.

   This is because of the special memory map of the PC-8401A. In a standard CP/M configuration, a BDOS error falls into address 00000H, which is re-routed by XSUB so that control is returned to XSUB.

   In the PC-8401A CP/M, address 00000H holds a jump to the system initializer when a ROM program is being executed. The CCP commands are handled as special ROM programs and, in this case, any BDOS error falls directly into the BIOS Warm Boot entry rather than passing through address 00000H.

   XSUB is not included with the PC-8401A.

CHAPTER 4

Memory configurations of the PC-8401A

SECTION 1

SUMMARY OF MEMORY CONFIGURATIONS

The CP/M on the PC-8401A supports two memory configurations:

1. The 32K CP/M configuration

   In this configuration, half of the available RAM of the PC-8401A is used as a RAM disk, and the other half is used as the Transient Program Area (TPA). Although a floppy disk or RAM cartridge is supported in this configuration, it is not a requirement.

2. The 64K CP/M configuration (with a RAM cartridge or a floppy disk)

   Either a floppy disk or a RAM cartridge is a prerequiste for this configuration. All of the built-in RAM is used as the TPA. The Floppy disk or RAM cartridge is used for file storage.

In each configuration, there are 4 modes that are automatically selected by the MENU software.

1. The RAM user mode

   This is the selected mode when a program is running in RAM. CP/M (more precisely BDOS) runs in this mode when called from a RAM based application program.

2. ROM user mode

   This is the selected mode when a program is running in ROM. CP/M (BDOS)runs in this mode when called from a ROM based application program.

3. CCP mode

   This is the selected mode when the CCP (MENU) is running.

4. Kernel mode

   This is the selected mode when BIOS is running. Interrupt routines also run in this mode.

SECTION 3

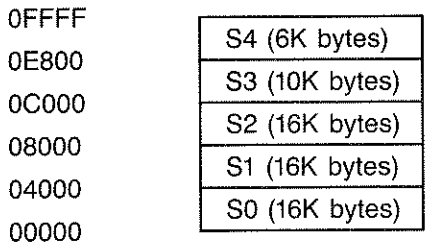
32K CP/M CONFIGURATION

In the 32K CP/M configuration, half of the 64K bytes of internal RAM are used as a RAM-disk. The other 32K bytes are utilized as the TPA for program execution, a Bios work area, and a communication area which is used to pass information between the different memory banks.

Programs in ROM can also be used in this mode. In this case, the 32K of RAM which was used as the TPA is now used for the variable data area of the program.

RAM SEGMENTATION

The 64K bytes of physical (built-in) RAM is divided into 5 segments as illustrated below:



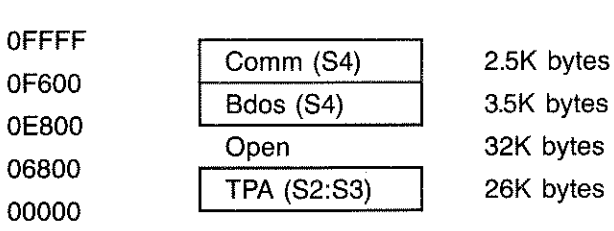
Note that the addresses in the above figure are not physical CPU addresses but are the logical memory addresses mapped to the various RAM chips.

Each memory segment (S0 through S4) can be mapped into a different CPU address space by programming the Memory Mapping Register (MMR). Details of the various MMR configurations will be discussed in later sections.

RAM USER MODE

In this mode, an application program is loaded from the RAM disk into TPA area and executed.

The memory segment (Sn) in the figure below indicates one of the physical RAM segments defined in the last section. Sm:Sn indicates that two physical RAM segments are concatenated. Segment Sm is placed into lower CPU address.



MMR value	*b6*	*b5*	*b4*	*b3*	*b2*	*b1*	*b0*
	0	1	0	1	0	x	x

The size of the TPA is 26K bytes, which is the same TPA size of a 31K CP/M when the CCP area is overwritten.

CP/M always stays in the CPU address space when an application program is running. It is possible to design a memory configuration so that CP/M runs in a different memory mode from that of the application program, however it causes interbank memory transfer to happen so many times (to pass the FCB between CP/M and the application program) that it is obviously inefficient and error prone and therefore should be avoided.

It is possible to merge the RAM user mode with the ROM user mode (see next section) in a 32K CP/M configuration. From the viewpoint of TPA size, there's no difference in running application programs from 08000H instead of 0100H. Non-standard TPA addresses would not pose a problem since most application programs which already exist for CP/M machines need more than 32K of TPA and also need a 25 line screen and therefore must be modified anyway.

The reason why the TPA needs to start at 0100H is that the program designed for a 32K CP/M configuration must also run in 64K CP/M configuration without modification.

ROM USER MODE

Cpu Address	Contents	
0FFFF		
0F600	Comm (S4)	2.5K bytes
0E800	Bdos (S4)	3.5K bytes
08000	Data (S2:S3)	26K bytes
00000	AP ROM	32K bytes

MMR value	*b6*	*b5*	*b4*	*b3*	*b2*	*b1*	*b0*
AP is in ROM #0	0	1	0	0	0	0	0
AP is in ROM #1	0	1	0	0	0	0	1
AP is in ROM #2	0	1	0	0	0	1	0
ROM cartridge AP	0	1	0	0	0	1	1

Application ROM (AP) programs run in this mode. The ROM is located at the lower half of the CPU address space. 26K bytes of RAM are provided for data storage and bookkeeping purposes for each application program.

The page in addresses 08000H through 080FFH is handled in a special manner. This page emulates the Zero Page which is normally located at 00000H through 000FFH in the usual CP/M memory configuration. The Zero Page at 08000H holds the same information as the standard CP/M Zero Page. When control is transfered to the ROM program, the default buffer is placed at 08080H, the default FCB is set at 0805CH, and the 2nd file name (if any) is set at 0806CH. Address 08000H holds a jump to the Reboot entry in the BIOS, and 08005H holds a jump to the BDOS entry in CP/M (these two jumps come to the BIOS through the Common area.)

CCP MODE

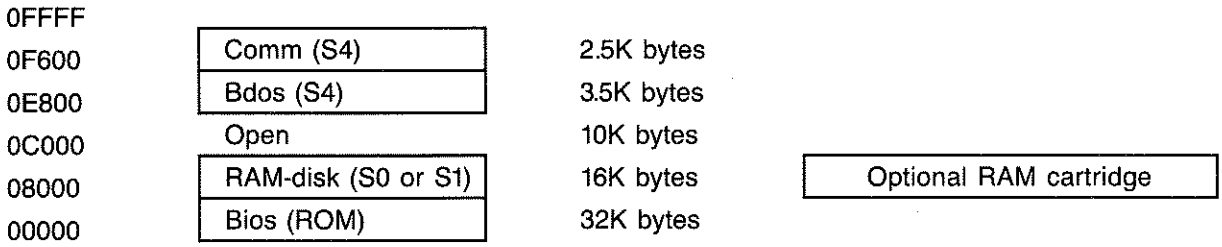
Cpu Address	Contents	
0FFFF		
	Comm (S4)	2.5K bytes
0F600		
	Bdos (S4)	3.5K bytes
0E800		
	TPA (S2:S3)	26K bytes
08000		
	CCP ROM	32K bytes
00000		

MMR value	*b6*	*b5*	*b4*	*b3*	*b2*	*b1*	*b0*
	0	1	0	0	0	0	0

The CCP (MENU) runs in the same memory mode as the ROM user mode. The physical RAM segment which becomes the TPA in the RAM user mode is relocated to 8000H in the CCP mode. The CCP loads the program into this area and switches the memory mode to the RAM user mode.

When initiating a ROM program, the CCP first sets up the Zero Page at 8000H, then switches the memory configuration to the ROM user mode, and finally transfers control to the program in ROM. The transfer address is stored in a fixed location in each ROM along with the name of the ROM program displayed by the menu screen of the CCP. The details of that fixed location are described elsewhere in this manual under ROM specifications.

KERNEL MODE



MMR value	*b6*	*b5*	*b4*	*b3*	*b2*	*b1*	*b0*
S0 access	0	0	0	0	0	0	0
S1 access	0	0	1	0	0	0	0
RAM cartridge	0	1	1	0	0	0	0
CRT access	1	x	x	0	0	0	0

The BIOS runs in this mode. The 32K bytes of RAM disk are divided into two 16K byte RAM segments and mapped into CPU addresses 08000H through 0BFFFH. The optional RAM cartridge is also divided into 2 16K byte banks and can be mapped in the same space. Note that the two 16K byte banks are handled together as one RAM-disk from the application programs' and the user's points of view.

In the kernel mode, there are several occasions where the BIOS needs to access the TPA RAM or an AP ROM that is placed outside the CPU addressing space:

1. Disk I/O request

   The transfer address is usually in the TPA RAM. In addition, there are occasions where a ROM application program requests CP/M to write data from that ROM to a file. In either case, the data is outside the CPU addressing space when in the kernel mode.

   Program loading is also made by this request which comes from the CCP.

2. Zero page access

   When reading the I/O Byte, or creating the default FCB after a command line was parsed by the CCP, etc.

3. String access.

   Some extended BIOS functions pass a pointer to a variable length string (or structure) that is to be manipulated. These strings are normally located outside the CPU addressing space when in the Kernel mode, and therefore require memory swapping.

The TPA access for disk I/O will be made using the sector buffer allocated in the Common area and a tiny routine which temporarily changes the mode into the same user mode that the disk I/O request was made. Sector data is then transferred between the buffer and the TPA.

Although it is possible to do the transfer while staying in the kernel mode (by temporarily changing the memory mapping register so that the TPA RAM is swapped into the CPU addressing space instead of the RAM disk) this is NOT recommended for these two reasons:

1. When the TPA RAM is placed at the upper half of the CPU addressing space, the highest 1K bytes of RAM are inaccessible since these bytes always contain the interbank communication area.

2. The transfer address requested by an application program needs to be mapped properly into the address specified by the current user mode, since the same physical RAM may be placed at 00000H in one mode (the RAM user mode,) and at 08000H in another mode (the ROM user mode.)

The accessing of the zero page can be done by writing another small routine in the BIOS work area, which temporarily switches to the user mode, and reads or writes a byte in memory specified by the HL register pair. String access can be resolved in a similar manner.

To summarize, keep in mind when writing CCP and BIOS code:

> The address passed by the application is the address in the mode under which the application program is running. The address may be mapped differently or may not even exist in the CPU addressing space while in the kernel mode.

BIOS CALLS

The BIOS is located outside of the CPU addressing space when the user program is running. BIOS calls are passed to the BIOS code through the common area. Since the user's stack area is swapped out of the CPU addressing space when the BIOS code is swapped into the addressing space, the BIOS needs its own local stack. The stack switching is performed by an interface code in the common area.

There are two types of BIOS entries:

One as defined in the CP/M manual (the standard BIOS), and one unique to The PC-8401A implementation of CP/M (the extended BIOS).

The CP/M defined BIOS entries are entirely compatible with standard CP/M and consist of 17 jump instructions that are located at the beginning of the Common Area (0F600H through 0F632H). A jump instruction to the Warm Boot entry is placed by the CCP at CPU address 00000H, which is also standard, so that any application program which refers to the jump instruction to find out the page number of the BIOS jump vectors will correctly reach the vectors of the PC-8401A CP/M.

An entry to extended BIOS functions is placed at CPU address 00010H. A call to this location with the appropriate function number in a certain register can be used to request the services of the extended BIOS. Application programs may use RST 2 instead of CALL 10 to save space, though either will work.

Application programs MUST NOT call routines in the BIOS ROM by directly switching memory banks.

SECTION 4

64K CP/M configuration

This mode allows application programs designed for larger CP/M environments (like 56K CP/M) to be used.

All of the built-in RAM except that used for the BDOS and the common area (a 6K area) are used as the TPA. Therefore, this configuration requires external file storage, which can be either floppy disk(s) or a RAM-Disk cartridge.

Note that programs designed for a 32K CP/M configuration can also run in this configuration.

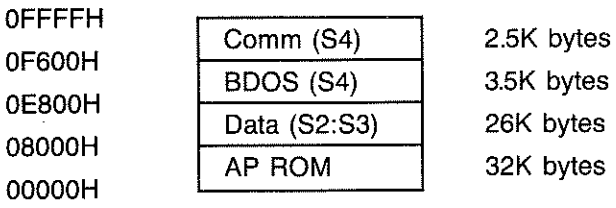
RAM USER MODE

CPU Address	Contents	
0FFFFH	Comm (S4)	2.5K bytes
0F600H	BDOS (S4)	3.5K bytes
0E800H	High TPA (S2:S3)	26K bytes
08000H	Middle TPA (S1)	16K bytes
04000H	Low TPA (S0)	16K bytes
00000H		

MMR value	*b6*	*b5*	*b4*	*b3*	*b2*	*b1*	*b0*
	0	1	0	0	1	x	x

The size of the TPA is 58K bytes, which is the same TPA size as a 63K CP/M when the CCP area is overwritten.

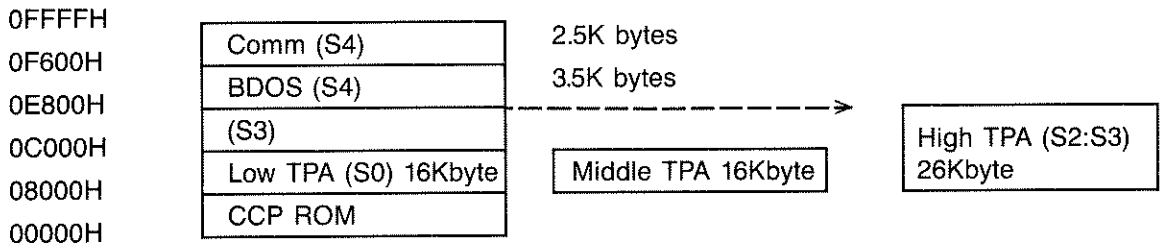
ROM USER MODE



MMR value	*b6*	*b5*	*b4*	*b3*	*b2*	*b1*	*b0*
AP is in ROM #0	0	1	0	0	0	0	0
AP is in ROM #1	0	1	0	0	0	0	1
AP is in ROM #2	0	1	0	0	0	1	0
ROM cartridge AP	0	1	0	0	0	1	1

The ROM user mode in the 64K CP/M configuration is exactly the same as in 32K CP/M configuration. Only 26K bytes of RAM is provided for the data area of the ROM program. In this mode, half of the available RAM is not used.

CCP MODE

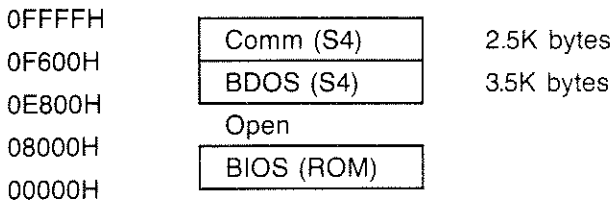


MMR value	*b6*	*b5*	*b4*	*b3*	*b2*	*b1*	*b0*
Low TPA access	0	0	0	0	0	0	0
Middle TPA access	0	0	1	0	0	0	0
High TPA access	0	1	0	0	0	0	0

The CCP in the 64K CP/M configuration handles the TPA by swapping one of the low, middle, or high TPA RAM segments into the CPU addressing space at 08000H through 0BFFFH. Since the loading of the application program is made in 128 byte increments, there is no chance that the DMA address would be set across the boundaries of any TPA segment.

The CCP needs its own bookkeeping area and stack area. Since RAM segment S3 is always in CPU address space regardless of the above TPA swapping, the highest portion of the S3 segment is used for this bookkeeping and stack.

KERNEL MODE



MMR value	*b6*	*b5*	*b4*	*b3*	*b2*	*b1*	*b0*
LCD access	0	x	x	0	0	0	0
CRT access	1	x	x	0	0	0	0

The same situation as in the 32K CP/M kernel mode exists here, and the same methods used there are used in this mode.

SECTION 5

MEMORY MAPPING REGISTER (MMR)

CPU ADDRESS SEGMENTATION

The CPU address is divided into 5 segments as illustrated below:

CPU Address	Segment Name	Physical Memory mapped in segment
0FFFFH	A4 (6K bytes)	Always S4
0E800H	A3 (10K bytes)	S3 or the optional CRT video memory
0C000H	A2 (16K bytes)	S0, S1, S2 or the low/high 16K bytes of the optional RAM cartridge
08000H	A1 (16K bytes)	S1, S3 or the high 16K bytes of one of the ROMs
04000H	A0 (16K bytes)	S0, S2 or the low 16K bytes of one of the ROMs.
00000H		

In each address segment, one of the physical memories listed at the right of the segment in the above figure is mapped.

The Memory Mapping Register (MMR) is used to perform the mapping.

BIT ASSIGNMENT OF MEMORY MAPPING REGISTER

The memory mapping register is a 7 bit port that controls how the ROM and RAM are mapped into the CPU addressing space. In this section, "bn" indicates the nth bit in the port (where the lsb is bit 0). "bm:bn" indicates bits from the mth bit through nth bit inclusive.

b1 and b0 — ROM Section

b1	*b0*	*ROM selection*	*Note*
0	0	ROM #0	Default selection
0	1	ROM #1	
1	0	ROM #2	
1	1	Optional ROM cartridge	

The bits, b1:b0 are used for ROM mapping. When a ROM is placed in the CPU addressing space, it is always mapped in the lower 32K bytes of the CPU addressing space. The bits, b1 and b0 in the MMR are used to specify which ROM is placed in the lower half of the CPU addressing space. Note that b1:b0 selects one of the ROMs that CAN be placed in the CPU addressing space. Whether or not the selected ROM is actually mapped into the CPU addressing space is determined by bits b3:b2.

b2 and b3 — Mapping for CPU addresses 00000H to 07FFFH

b3	*b2*	*ROM/RAM*	*Cell addresses*	*Note*
0	0	ROM	00000H to 07FFFH	A ROM selected by b1:b0 is mapped. At startup, b3:b2 is reset to this mode.
0	1	RAM	00000H to 07FFFH	
1	0	RAM	08000H to 0FFFFH	
1	1	None	Invalid	

Bits b3 and b2 determine which physical memory is mapped into CPU segment A0 and A1 (ie: CPU address 00000H through 07FFFH.

b4 and b5 — Mapping for CPU addresses 08000H to 0BFFFH

b5	*b4*	*ROM/RAM*	*Cell addresses*	*Note*
0	0	RAM	00000H to 03FFFH	Default mapping
0	1	RAM	04000H to 07FFFH	
1	0	RAM	08000H to 0BFFFH	
1	1	RAM cartridge	00000H to 03FFFH or 04000H to 07FFFH	A port in the cartridge determines which of the 16K memories is actually mapped.

Bits b5 and b4 determine the physical memory mapped into CPU segment A2 (CPU address 08000H through 0BFFFH.

b6 — Mapping for CPU addresses 0C000H to 0E7FFH

b6	*ROM/RAM*	*Cell addresses*	*Note*
0	RAM	0C000H to 0E7FFH	Default mode.
1	CRT Video RAM	00000H to 01FFFH	Memory in the CRT interface is mapped into CPU addresses 0C000H through 0DFFFH. CPU addresses 0E000H through 0E7FFH are undefined.

Bit b6 determines the physical memory mapped into CPU addresses 0C000H through 0E7FFH. The high 12K bytes of RAM segment S2 (RAM cells from 0C000H through 0E7FFH) or the optional video memory for the CRT can be mapped into this addressing space. Since the video memory is 4K bytes long, the memory occupies CPU address 0C000H through 0DFFFH, and 0E000H through 0E7FFH is left open.

CPU addresses 0E800H through 0FFFFH are always occupied by physical RAM segment S4 (the RAM whose cell address ranges from 0E800H through 0FFFFH).

One physical memory segment can be mapped into more than one CPU addressing space segment. This is allowed just to simplify memory mapping hardware.

When programming the MMR in the 32K CP/M mode, do not map the RAM disk memory segment (S0 and S1) into the CPU addressing space except while in the kernel mode. This is to prevent the contents of the RAM-disk from being accidentally destroyed by application programs.

SECTION 6

SELECTING CONFIGIRATIONS

Upon the first startup, the 32K CP/M mode is selected. To change the mode to the 64K CP/M mode, the user needs to invoke the CCP command "MODE", which is one of subcommands of the OPTION command.

In order to use the 64K CP/M mode, either floppy disk(s) or a RAM-Disk cartridge are prerequisites. Since all the files in the built-in RAM-disk will be lost when the 64K CP/M mode is selected, the user must save all the files from the built-in RAM disk to a floppy disk or the RAM cartridge prior to using the MODE command.

The MODE command is a toggle function. To return to the 32K CP/M mode, the user must issue the MODE command again.

The PC-8401A always keeps track of the current CP/M mode, and when the power is turned on, the same CP/M mode (as had been selected at the time of the last power down) is automatically restored.

Under certain circumstances, the PC-8401A is forced into the 32K CP/M mode:

1. When the system configuration is changed.

   At start up, the PC-8401A checks for the peripheral devices that are connected. If the configuration has been changed since the last power down, the PC-8401A performs a cold start which selects the 32K CP/M mode.

2. When SHIFT and STOP keys are pressed at start-up.

   If the SHIFT and STOP keys are simultaneously held down at start-up, the PC-8401A performs a cold start and selects the 32K CP/M mode.

   This is mainly used to escape from an infinite loop which may be caused by hardware or software defects. The PC-8401A normally resumes execution of an application program stopped by power-down when power is again applied. The program resumes executing at the place it was at when the power-down occurred. If the program entered an infinite loop, the only way to regain control would be by means of the SHIFT + STOP keys at start-up.

SECTION 7

BDOS

The PC-8401A uses the standard CP/M 2.2 BDOS with only minor modification. The BDOS is copied from ROM into RAM and executed in RAM. This is because some of the existing CP/M application programs patch the BDOS.

The BIOS needs to copy the BDOS from ROM to RAM every time a warm boot request is made.

The modification of the BDOS has been made to support the ROM user mode.

The BDOS makes reference to a few fixed locations in Page Zero, namely: the I/O Byte and the default DMA address. The I/O Byte is usually located at 00003H, and the DMA address is usually located at 00080H. In the RAM user mode, both are at their standard locations no matter which of the CP/M modes is currently selected. However, in the application ROM mode, these two must be relocated to 08003H and 08080H since addresses 00003H and 00080H are now addressing ROM memory.

For the aforementioned reason, a few patches have been made to the BDOS instructions which refer to the I/O Byte and the default DMA addresses so that these addresses are altered when the ROM user mode is selected.