TANDY®
Service Manual

PORTABLE DISK DRIVE

Catalog Number: 26-3808

CUSTOM MANUFACTURED FOR RADIO SHACK, A DIVISION OF TANDY CORPORATION

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1. INTRODUCTION

The TANDY Portable Disk Drive is a stand-alone 3.5-inch micro floppy disk drive. It interfaces to the Portable Computer through the RS-232C port and may be powered by batteries for maximum portability.

Its compactness and light weight enable it to be carried along with the Portable Computer. Although tiny in size, a 3.5-inch diskette can store up to 100,000 bytes of data.

2. GENERAL SPECIFICATIONS

1. Storage capacity (Formatted)
   Per disk .... 101.12K bytes
   Per track .... 2,560 bytes
   Per hard sector .... 1,280 bytes

2. Disk
   Number of surfaces 1
   Number of memory blocks 80
   Total number of tracks 40
   Total number of hard sectors 80

3. Recording systems
   Recording method .... FM
   Recording density .... 4,064 BPI
   Track density .... 67.5 TPI
   Data transfer rate .... 125K bits/sec.

4. Process time
   Average access time .... 820 ms
   Track to track .... 60 ms
   Settling time .... 20 ms
   Motor start time .... 1 sec.

5. Rotational speed .... 300 rpm

6. Number of Index 2

7. Power sources .... 4 AA Alkaline batteries
   (Cat. No. 23-552) or
   AC Adapter (Cat. No. 26-3804)

8. Power consumption : Operating .... 1.5 W
   : Waiting .... 0.16 W
   (1) Battery life : Continuous Read/Write .... Minimum 2 hours
   : Waiting only .... Minimum 10 hours
   (2) Low Battery : Alarm lamp average voltage ...... 4.1 V
   : Power down average voltage 3.7V

9. Dimensions .... 5-1/4" x 6-13/32" x 2-1/8"
   133 (W) x 163 (L) x 54 (H) mm

10. Weight .... 1 lb 14 oz 850 grams
   (Including 4 batteries)

11. Media used .... Single sided 3.5-inch micro
   floppy disk

12. Interface RS-232C
   Transfer rate : Booting .... 9600 bits/sec.
   : Operating .... 19200 bits/sec.

3. DISASSEMBLY INSTRUCTIONS

Upper case ass'y

Disk holder ass'y

Disk holder spring

Disk in/out bar

DC motor

Snap ring E2

Pad arm ass'y

Pad arm shaft ass'y

Power switch cover

Mechanical body with PCB

Lower case ass'y
with battery contact ass'y
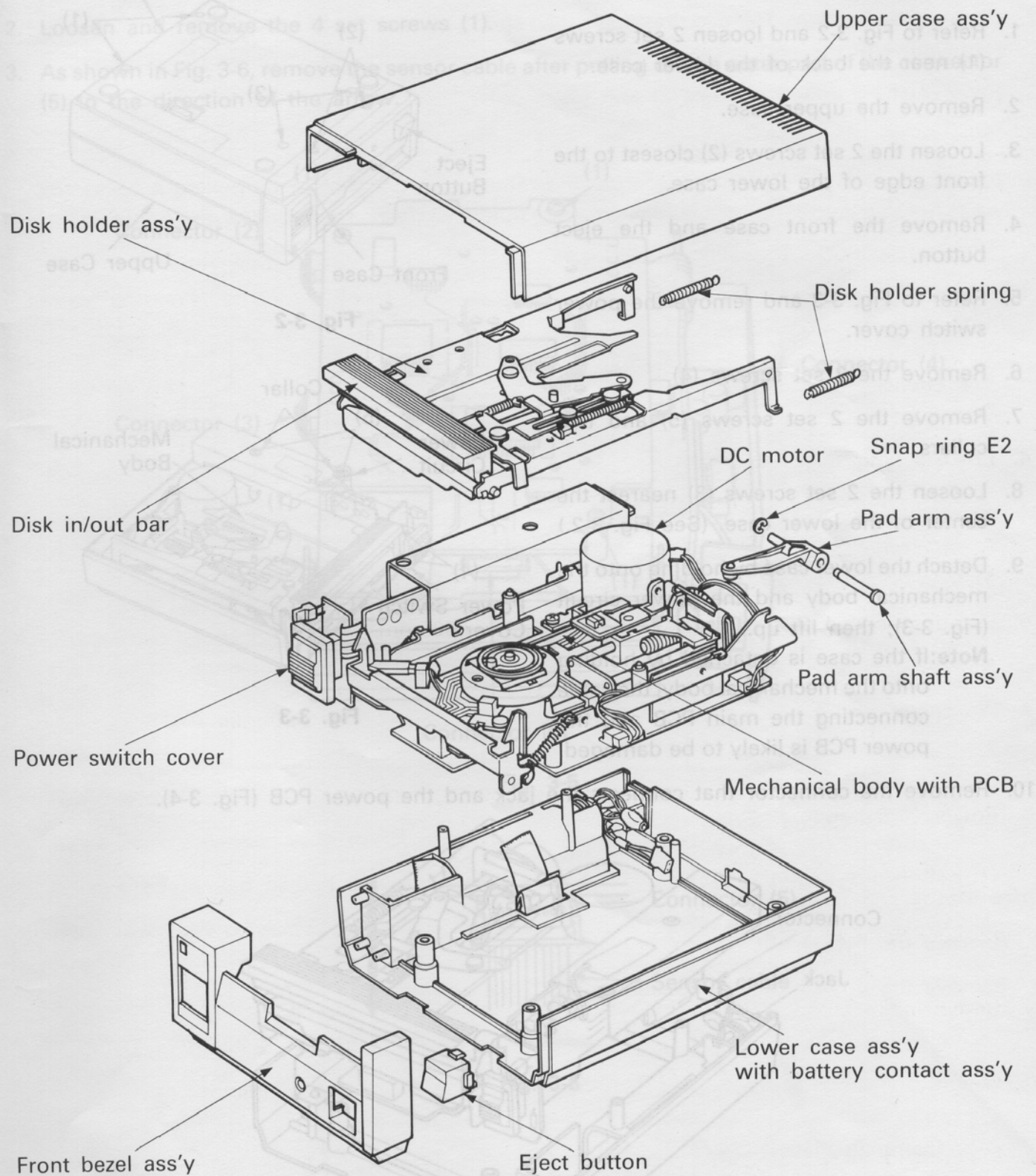
Front bezel ass'y

Eject button

Fig. 3-1

3-1. Disassembly

Case

1. Refer to Fig. 3-2 and loosen 2 set screws (1) near the back of the lower case.

2. Remove the upper case.

3. Loosen the 2 set screws (2) closest to the front edge of the lower case.

4. Remove the front case and the eject button.
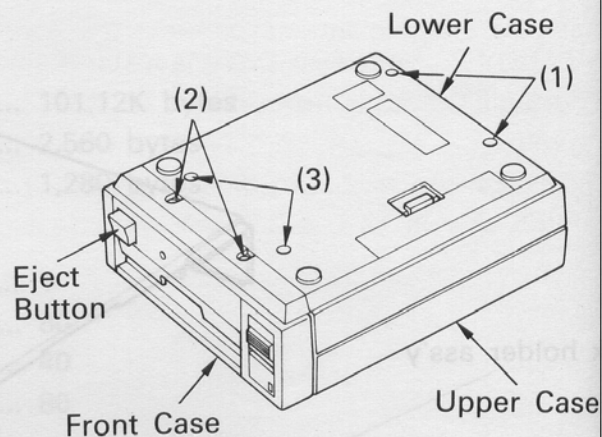
5. Refer to Fig. 3-3 and remove the power switch cover.

6. Remove the 2 set screws (4).

7. Remove the 2 set screws (5) and two collars.

8. Loosen the 2 set screws (3) nearest the center of the lower case. (See Fig. 3-2.)

9. Detach the lower case by holding onto the mechanical body and the power circuit (Fig. 3-3); then lift up.
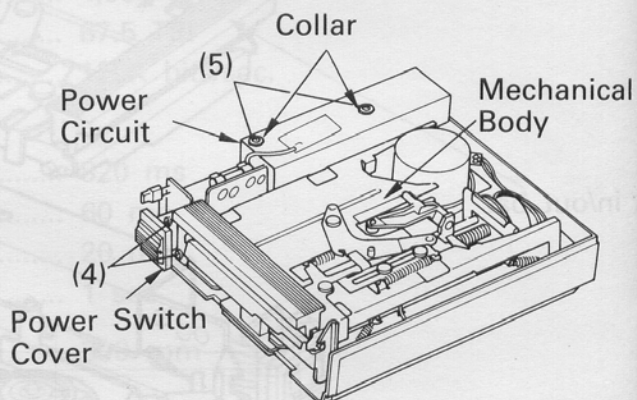
   Note: If the case is detached by holding onto the mechanical body, the cable connecting the main PCB and the power PCB is likely to be damaged.

10. Remove the connector that connects the jack and the power PCB (Fig. 3-4).

Lower Case

(1)

(2)

(3)

Eject Button

Front Case

Upper Case

Fig. 3-2

Collar

(5)

Power Circuit

Mechanical Body

(4)

Power Switch Cover

Fig. 3-3

Connector

Jack
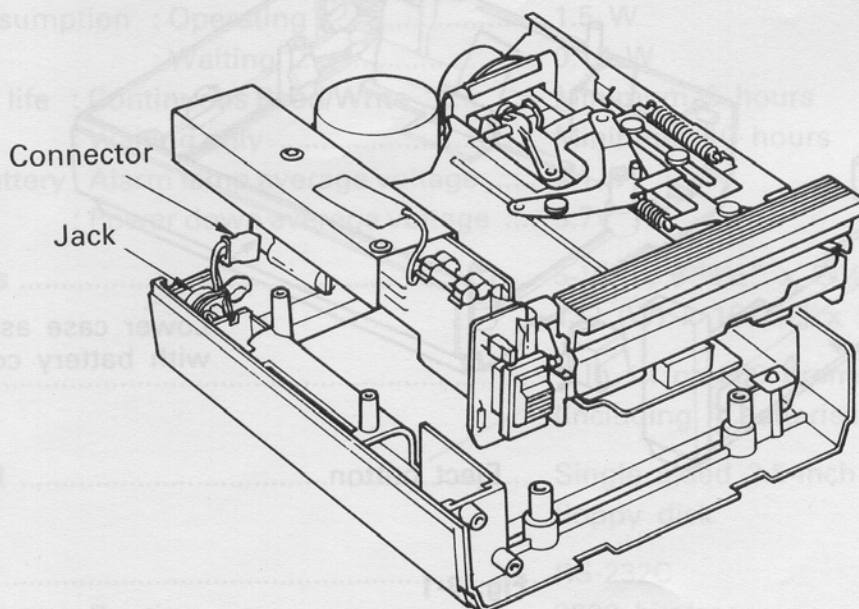
Fig. 3-4

PCB

1. Refer to Fig. 3-5 and disconnect the 4 connectors (2), (3), (4) and (5).

2. Loosen and remove the 4 set screws (1).

3. As shown in Fig. 3-6, remove the sensor cable after pulling off the outer part of the connector (5) in the direction of the arrow.
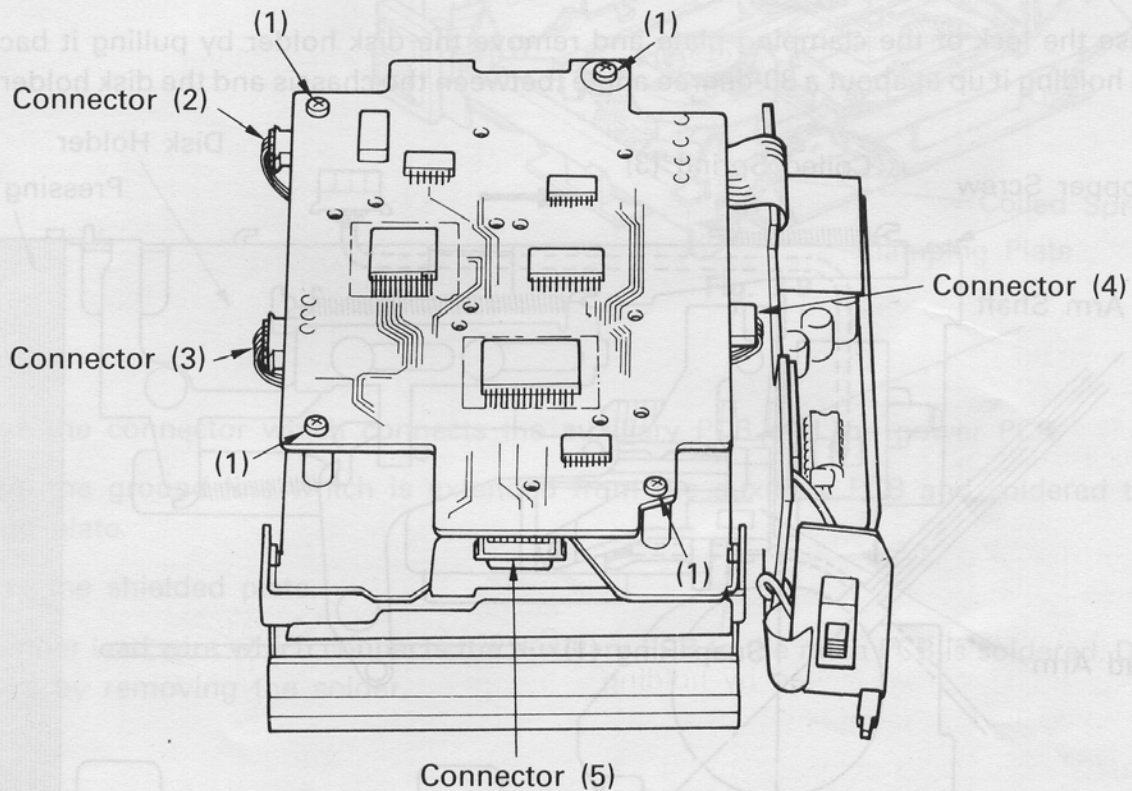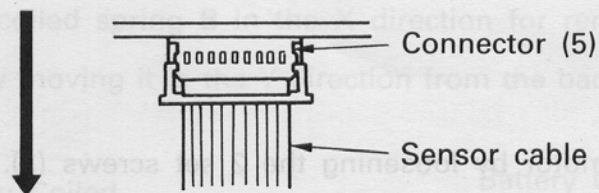
Fig. 3-5

Fig. 3-6

Disk Holder

1. Remove the snap ring (1) and pull out the pad arm shaft (Fig. 3-7).

2. Remove the pad arm. The pad pressing coiled spring under the pad arm will be automatically removed with the pad arm.

3. Remove the 2 coiled springs (2) and (3).

4. Remove the 2 stopper screws.

5. Release the lock of the clamping plate and remove the disk holder by pulling it backward while holding it up at about a 30-degree angle (between the chassis and the disk holder.) (Fig. 3-8).
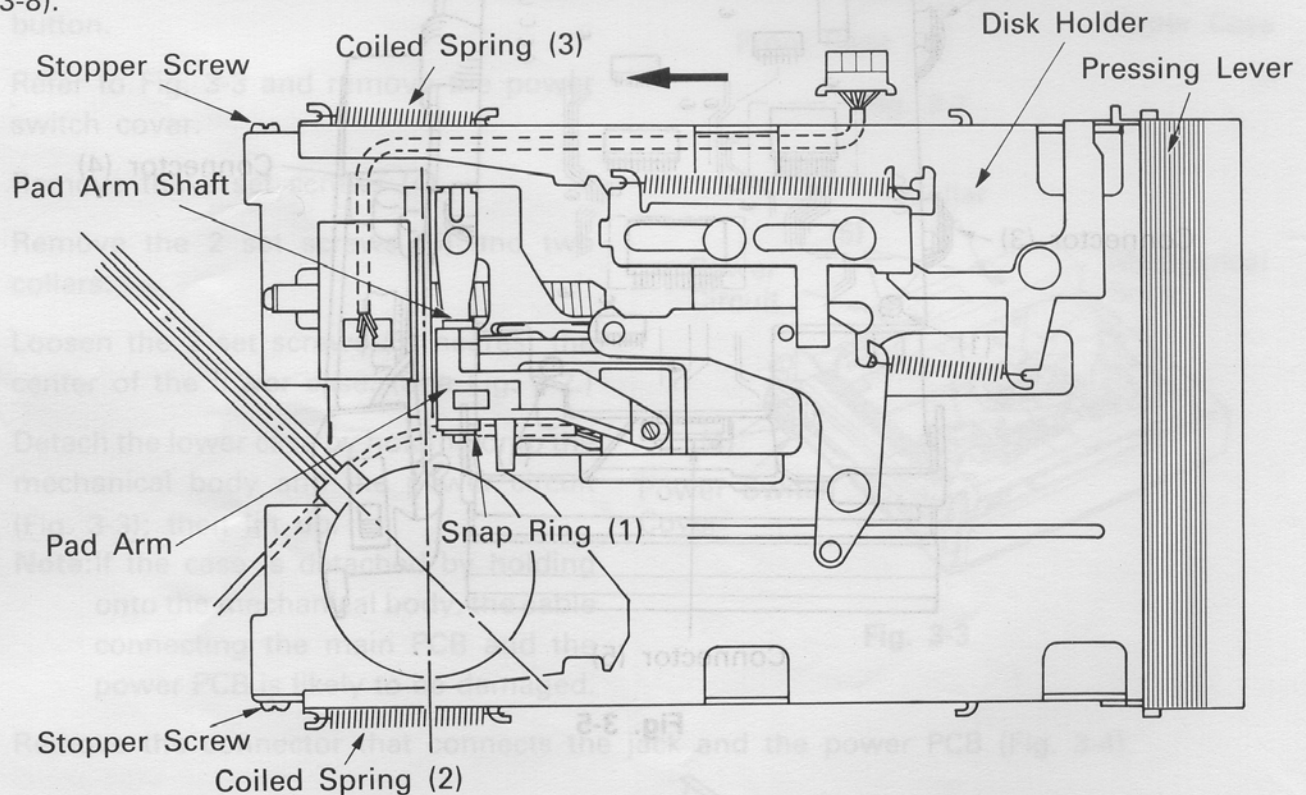
Fig. 3-7

Drive Motor

1. Remove the belt.

2. Remove the drive motor by loosening the 2 set screws (2).
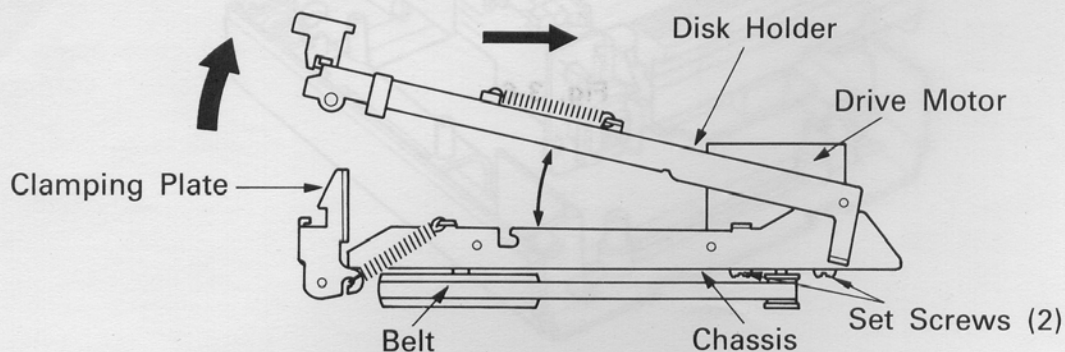
Fig. 3-8

Clamping Plate

1. Remove the 2 coiled springs on both sides in the front section of the unit.

2. Remove the clamping plate.
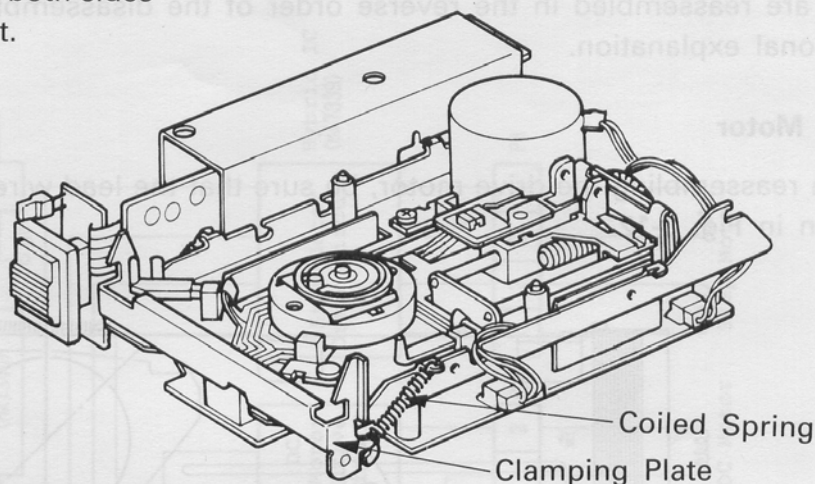
Fig. 3-9

PCB

1. Remove the connector which connects the auxiliary PCB and the power PCB.

2. Remove the ground line which is extended from the auxiliary PCB and soldered to the shielded plate.

3. Remove the shielded plate.

4. The jumper lead wire which connects the auxiliary PCB to the main PCB is soldered. Detach the wire by removing the solder.

Battery Contact

1. Remove the battery cover on the back of the lower case.

2. Move battery contact A in the X direction for removal (Fig. 3-10).

3. Move the jack and battery coiled spring B in the X direction for removal.

4. Remove battery contact C by moving it in the Y direction from the back of the lower case (Fig. 3-11).
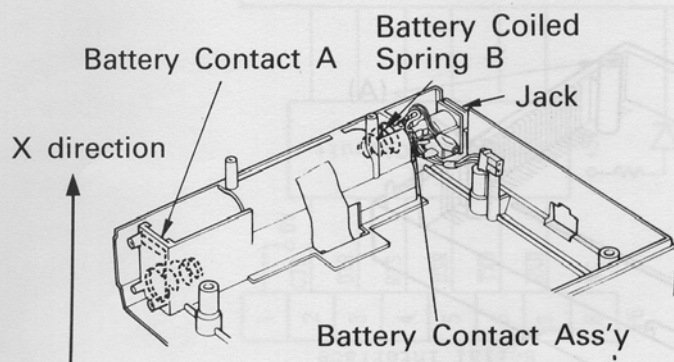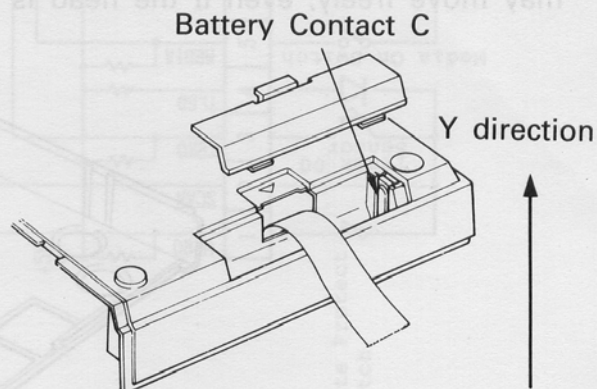

Fig. 3-10

Fig. 3-11

3-2. Reassembly

Parts are reassembled in the reverse order of the disassembly. The following items require additional explanation.

Drive Motor

When reassembling the drive motor, be sure that the lead wire is positioned at a 45° angle as shown in Fig. 3-12.
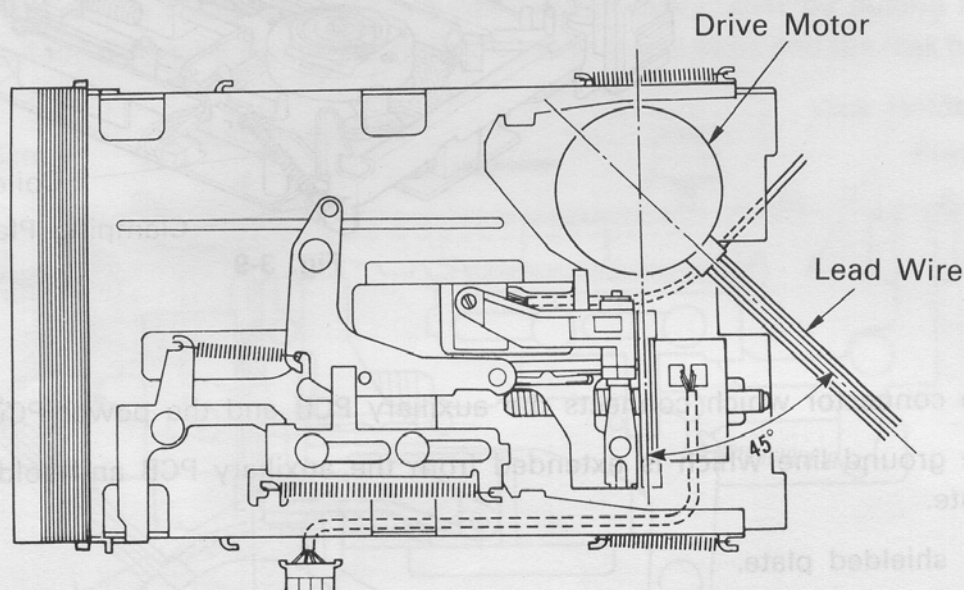
Fig. 3-12

IMPORTANT:

- Shielded Wire of Head
  Position the shielded wire so that it will not stretch when the head is moved to the center, and so that it will not apply excessive force to the head when the head is moved to the outermost periphery (or the position of Track 0).

- Case
  Do not let the legs (A) of the upper case interfere with the movement of the shielded wire of the head (Fig. 3-13). Also, be sure to provide sufficient length to the shielded wire so that it may move freely, even if the head is moved to the center.
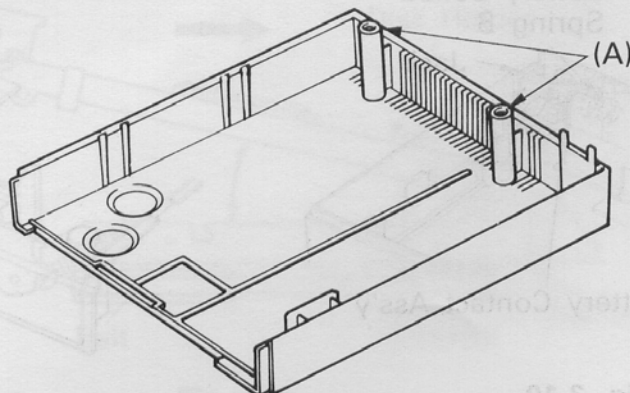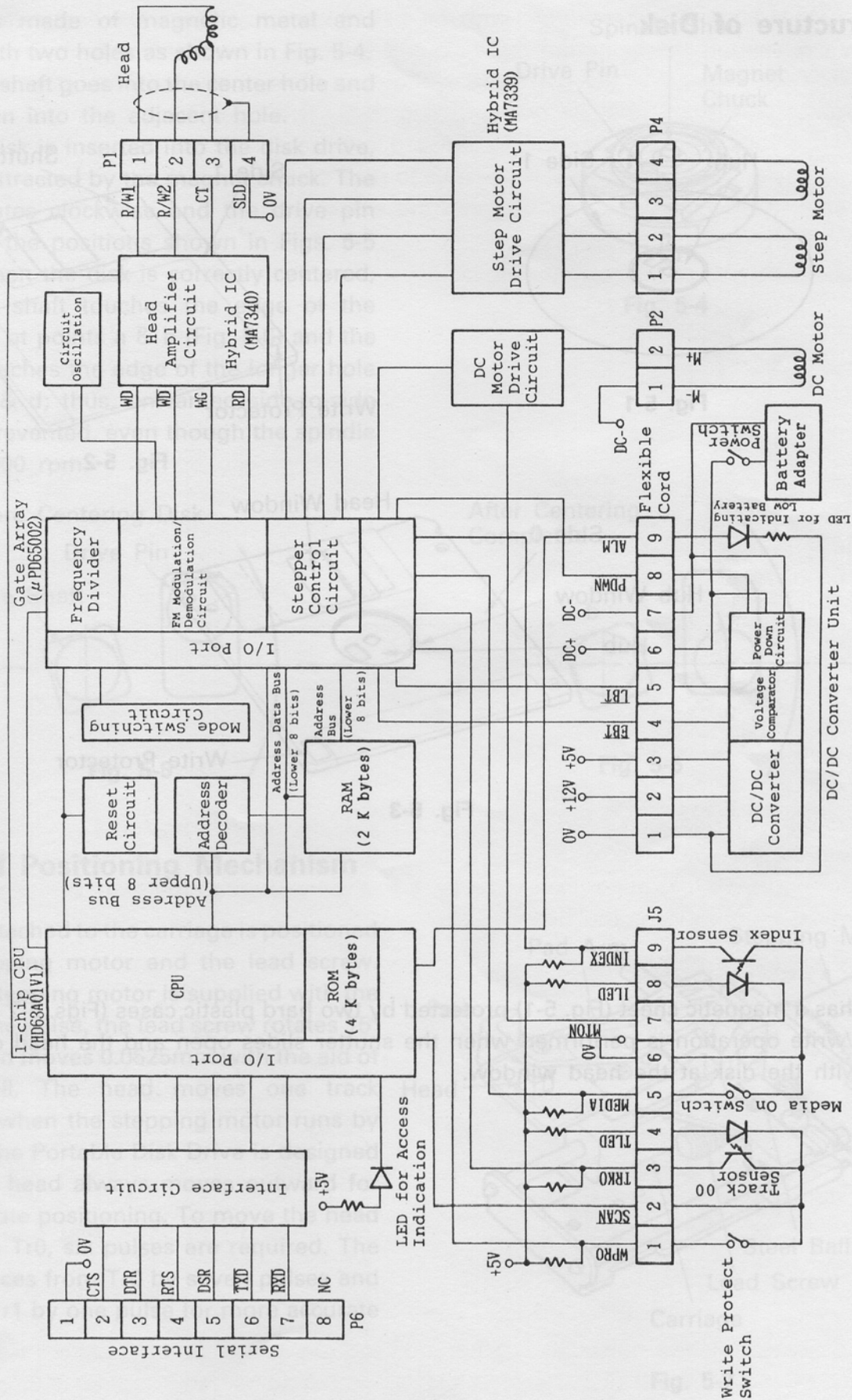
Fig. 3-13

4. BLOCK DIAGRAM

Fig. 4-1

5. PRINCIPLES OF MECHANICAL OPERATION
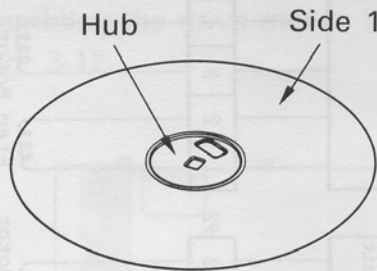
5-1. Structure of Disk
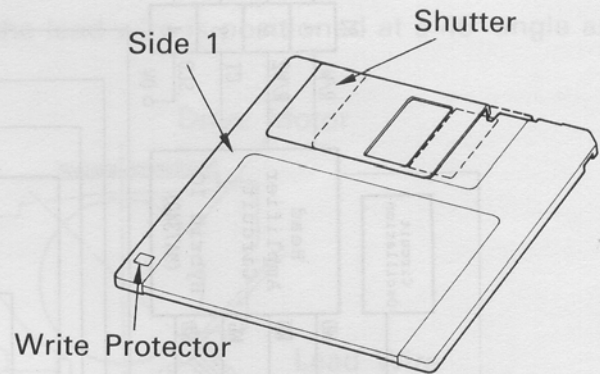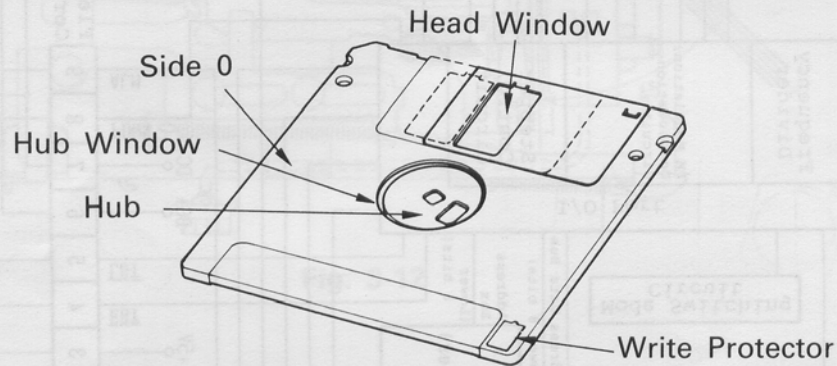

Fig. 5-1

Fig. 5-2

Fig. 5-3

The disk has a magnetic sheet (Fig. 5-1) protected by two hard plastic cases (Figs. 5-2 and 5-3). The read/write operation is performed when the shutter slides open and the head comes in contact with the disk at the head window.

5-2. Disk Driving Mechanism

The hub is made of magnetic metal and provided with two holes as shown in Fig. 5-4. The spindle shaft goes into the center hole and the drive pin into the adjacent hole.

When the disk is inserted into the disk drive, the hub is attracted by the magnet chuck. The spindle rotates clockwise and the drive pin moves into the positions shown in Figs. 5-5 and 5-6. When the disk is correctly centered, the spindle shaft touches the edge of the square hole at points a & b (Fig. 5-6) and the drive pin touches the edge of the longer hole at points c & d; thus, unwanted side-to-side motion is prevented, even though the spindle rotates at 300 rpm.

Fig. 5-4

Before Centering Disk

Fig. 5-5

After Centering Completed
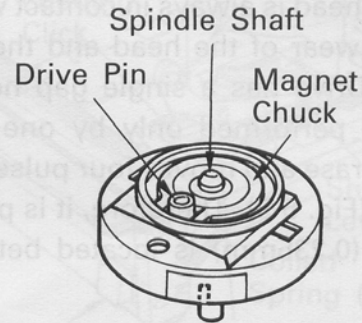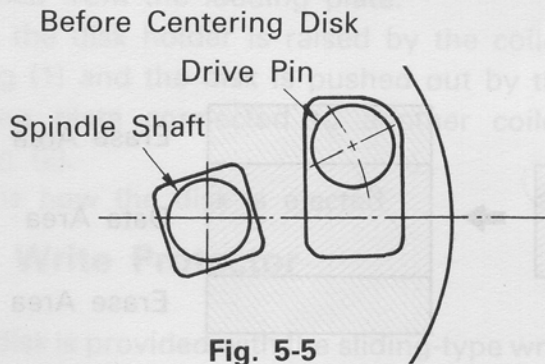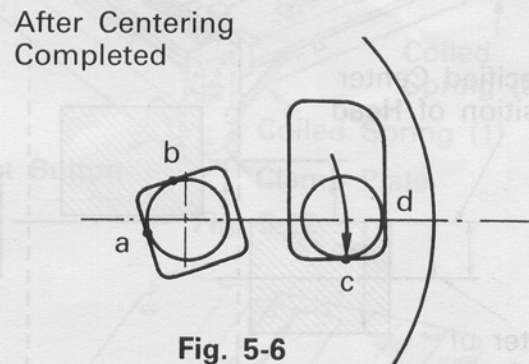
Fig. 5-6

5-3. Head Positioning Mechanism

The head attached to the carriage is positioned by the stepping motor and the lead screw. When the stepping motor is supplied with the power of one pulse, the lead screw rotates 15° and the head moves 0.0625mm with the aid of a steel ball. The head moves one track (0.375mm) when the stepping motor runs by six steps. The Portable Disk Drive is designed so that the head always moves outward for more accurate positioning. To move the head from Tr1 to Tr0, six pulses are required. The head advances from Tr0 by seven pulses and returns to Tr1 by one pulse for more accurate positioning.

Fig. 5-7

-11-
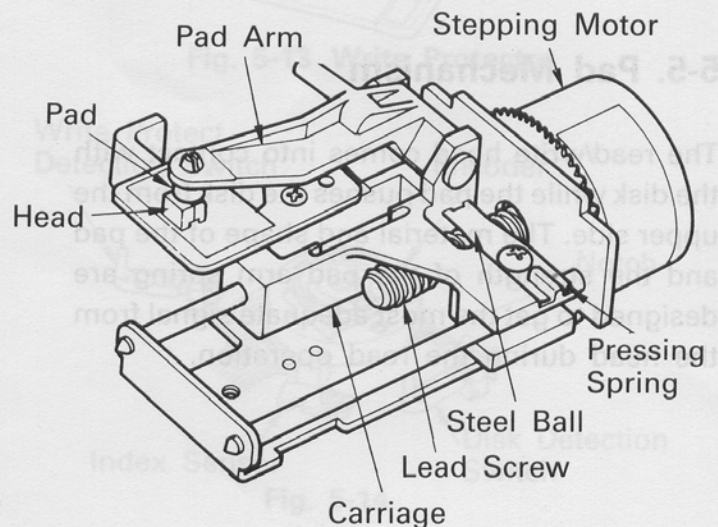
5-4. Structure of Read/Write Head

The read/write head is always in contact with the disk by means of a pad. The design of the head minimizes the wear of the head and the disk, and facilitates data reading from the disk. The Portable Disk Drive has a single gap head without an erase gap; the read, write and erase operations are performed only by one gap (Fig. 5-8). The head moves two pulses inward (0.125mm) to erase and moves four pulses outward to erase; then it moves two pulses inward to write the data (Fig. 5-9). Therefore, it is possible to read the data even if tracking is off, because the data area (0.235mm) is located between the erase areas.

Fig. 5-8

Fig. 5-9

5-5. Pad Mechanism

The read/write head comes into contact with the disk while the pad pushes the disk from the upper side. The material and shape of the pad and the strength of the pad arm spring are designed to get the most adequate signal from the head during the read operation.
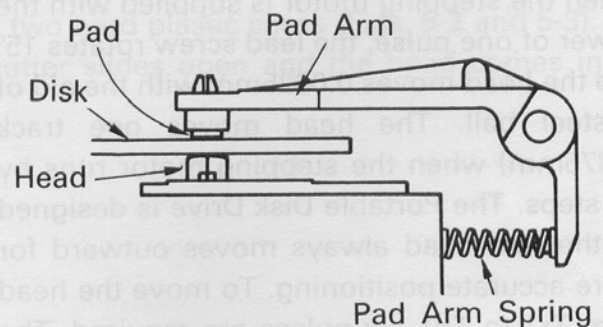
Fig. 5-10

5-6. Disk Eject Mechanism

When the disk is inserted into the disk holder, the loading plate pushes the shutter lever (Fig. 5-11). The shutter lever moves the shutter lever shaft so that it opens the shutter of the disk.

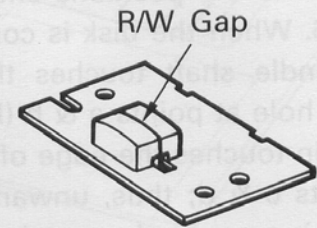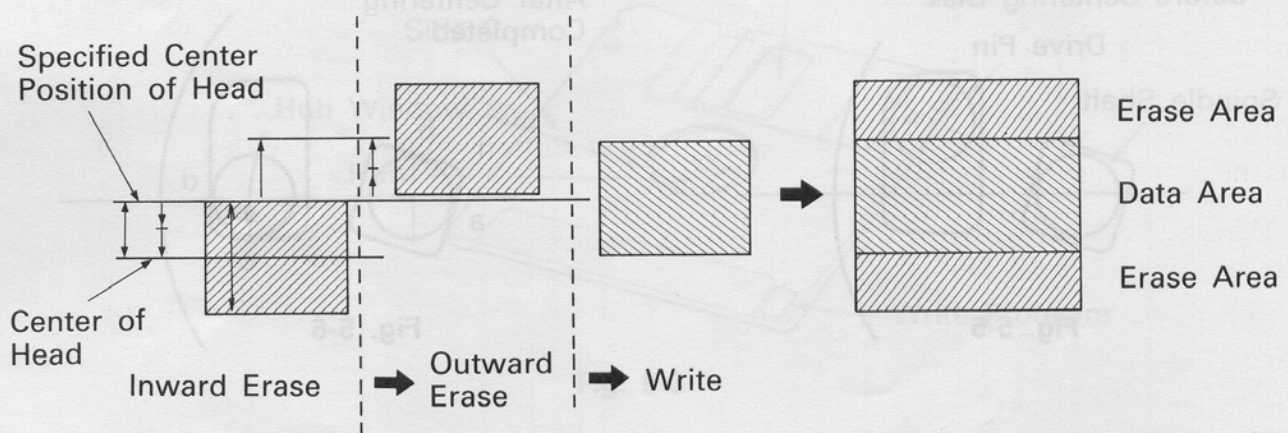When the disk is inserted all the way into the holder, the loading click and loading plate engage with each other and are locked into position. By pushing the disk in/out lever downward, the clamp plate and cylindrical convex part of the disk holder engage with each other and are locked into position.

When the eject button is pressed, the clamp plate is released from the cylindrical convex part of the disk holder and the loading click is released from the loading plate.

Then the disk holder is raised by the coiled spring (1) and the disk is pushed out by the loading plate connected to another coiled spring (2).

This is how the disk is ejected.
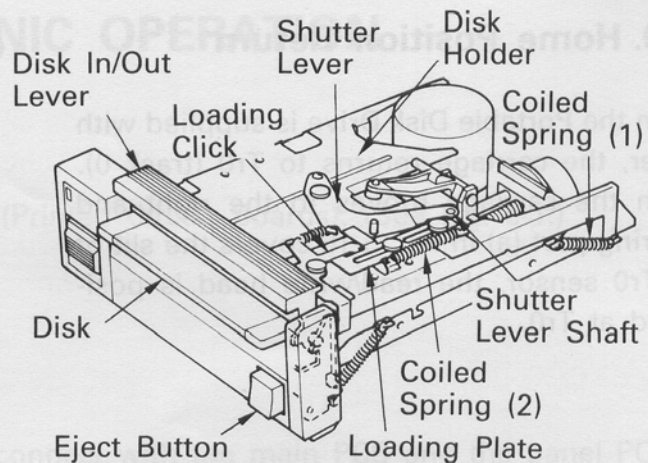
Fig. 5-11
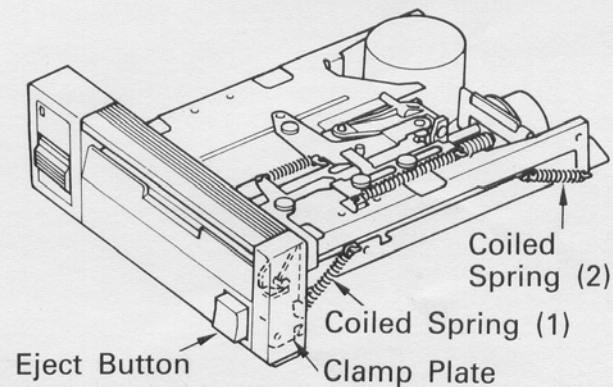
Fig. 5-12

5-7. Write Protector

The disk is provided with the sliding-type write protector (Fig. 5-13).

When this shutter slides open, the disk is in a state of write protection. The Portable Disk Drive detects this window with the write protect detection switch.
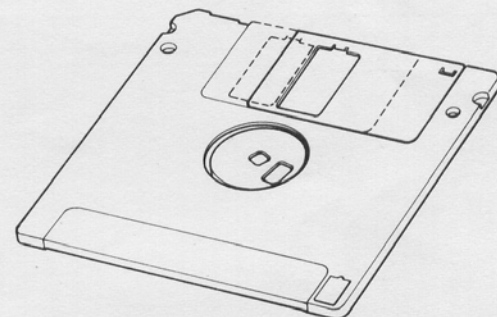
Fig. 5-13 Write Protector

5-8. Index

The Portable Disk Drive requires an index signal for read/write operations.

To detect the index signal, an index sensor searches for a big notch and a small one provided on the side face of the encoder (Fig. 5-14).
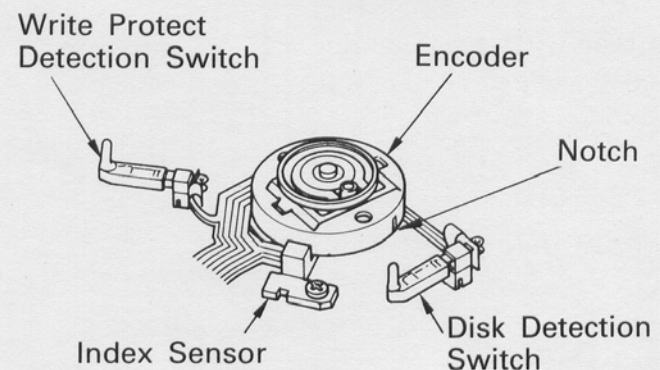
5-9. Disk Detection

Fig. 5-14

When the disk is inserted and locked into position, the disk detection switch is pressed by the disk. This switch detects whether or not a diskette is inserted in the Portable Disk Drive.

5-10. Home Position Return

When the Portable Disk Drive is supplied with power, the carriage returns to Tr0 (track 0). When the carriage moves to the right and covering part (a) in Fig. 5-15 covers the slit of the Tr0 sensor, the read/write head is positioned at Tr0.

Covering part   Tr0 Sensor

(a)

Carriage

Fig. 5-15

6. PRINCIPLES OF ELECTRONIC OPERATION

6-1. Electronic Components

The electronic section consists of four PCBs (Printed Circuit Boards). (See Fig. 6-1.)

- Main PCB
- Auxiliary PCB
- Panel PCB
- DC-DC Unit

The auxiliary PCB has two flat cables which connect with the main PCB and the panel PCB respectively. It also has the connector which connects with the DC-DC unit.

Interface Cable

See page 18 regarding the connection with the computer

K9 Magnetic Head
- RE R/W1
- WH R/W2
- YE CT

K6 DC Motor (−) (+)

K7 Pulse Motor
- White PM1
- Red RE PM2
- Blue BE PM3
- Yellow YE PM4

K8 Sensor Cable
1	WPRO
2	SCAN
3	TRK0
4	TLED
5	MEDIA
6	0V
7	MTON
8	ILED
9	INDEX

J1   J3   J4   P5

P1
1	R/W1
2	R/W2
3	CT
4	SLD

P3
| 1 | M− |
| 2 | M+ |

P4
1	PM1
2	PM2
3	PM3
4	PM4

J5
1	WPRO
2	SCAN
3	TRK0
4	TLED
5	MEDIA
6	0V
7	MTON
8	ILED
9	INDEX

J6
1	0V
2	CTS
3	DTR
4	RTS
5	DSR
6	TXD
7	RXD
8	

K1 Main PCB
1	0V
2	+12V
3	+5V
4	EBT
5	LBT
6	DC+
7	DC−
8	PDWN
9	ALM

(mating:)
1	0V
2	+12V
3	+5V
4	EBT
5	LBT
6	DC+
7	DC−
8	PDWN
9	ALM

K4 DC-DC Unit — P7
1	PDWN
2	DC−
3	DC+
4	LBT
5	EBT
6	+5V
7	+12V
8	0V

J7
1	PDWN
2	DC−
3	DC+
4	LBT
5	EBT
6	+5V
7	+12V
8	0V

K5 Panel PCB
11	+5V
12	ALM
13	DC−
14	DC+
15	B−

1	+5V
2	ALM
3	DC−
4	DC+
5	B−

K2 Aux. PCB

P9
| 1 | DC+ |
| 2 | B− |

K3 Battery Contact — J9
| 1 | DC+ |
| 2 | B− |

J11
| 1 | AP+ |
| 2 | AP− |

AC Adapter

Fig. 6-1 Connection Diagram

6-2. Main PCB

The main PCB controls the entire system and consists of one interface circuit, 1-chip CPU, the gate array, two hybrid ICs (MA7339 & MA7340), the RAM, one oscillation circuit, reset circuit, and address decoder.

(1) Interface Circuit

Fig. 6-2. is an input and output circuit which shows the connection with a host (for example MODEL 100) by a pseudo RS-232C interface. (See Fig. 12-1 on page 70 for the overall circuit drawing.)
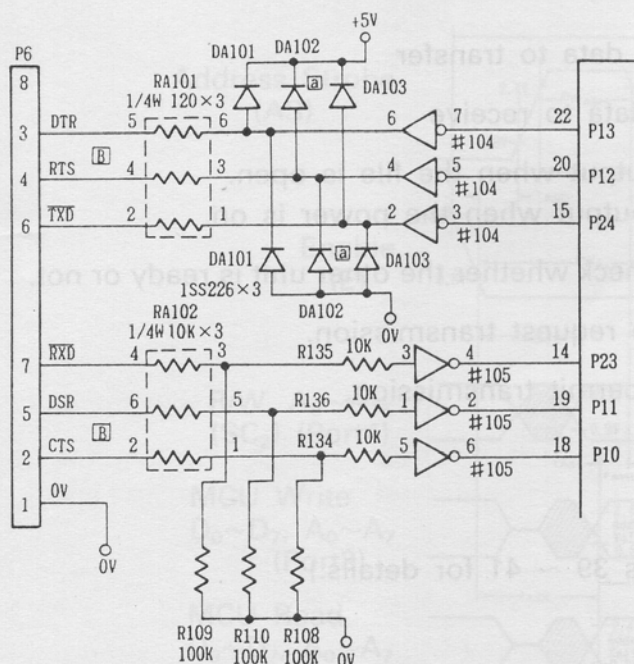
RA101 is a protective resistor for output short.
DA101 to DA103 are diodes to protect the IC #104 from latch-up.
RA102 is a protective resistor; the input voltage can be used with a variation of up to ±12V.
R108 to R110 are pull-down resistors.
R134 to R136 are current-limit resistors for IC #105 to prevent latch-up.

Fig. 6-2

- **Electrical Characteristics**

  Output $V_{OH} \approx 4.5V$ ($I_{OH} = -2.5mA$) $V_{OH} \approx 5 + 0.2 I_{OH}$

  $\qquad\qquad V_{OL} \approx 0.5V$ ($I_{OL} = 3mA$) $V_{OL} \approx 0.16 I_{OL}$

  Input $6V < V_{IH} < 15V$ $I_{IH} \approx (V_{IH} - 4.0)/1K$ (mA)

  $\qquad\qquad -15V < I_{IL} < 1V$ $I_{OL} \approx (-0.7 - V_{IL})/1K$

  $\qquad\qquad\qquad\qquad\qquad$ (where $-15 < V_{IL} < -0.7$)

  $\qquad\qquad\qquad I_{OL}$ $100\mu A$

  $\qquad\qquad\qquad\qquad\qquad$ (where $-0.7 < V_{IL} < 1$)

The sequence of the signal conforms to RS232C except the electrical characteristics.

● Connection with Host

```
   3 ← R x D ─────────────╲   ╱───────────── R x D → 7
   2 → T x D ──────────────╲ ╱────────────── T x D ← 6
   5 ← C T S ───────────────╳─────────────── C T S → 2
   4 → R T S ──────────────╱ ╲────────────── R T S ← 4
   6 ← D S R ─────────────╱   ╲───────────── D S R → 5
  20 → D T R ────────────╲   ╱───────────── D T R ← 3
   7 ↔ G N D ──────────────────────────────── G N D ↔ 1
      (HOST)                                    (SLAVE)
```
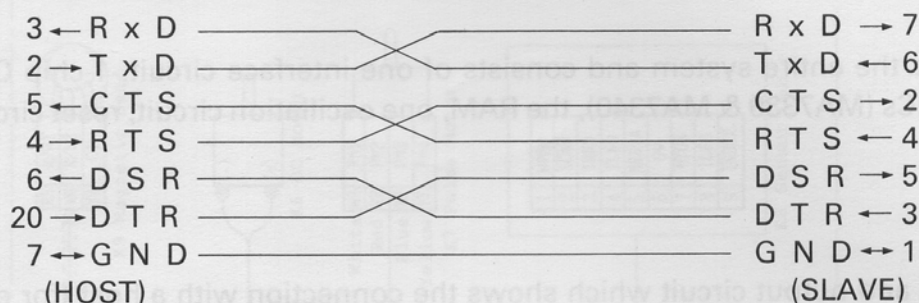
● Signal Name and Function

TxD Transfer Data: Output of serial data to transfer

RxD Receive Data: Input of serial data to receive

DTR Data Terminal Ready: Host – active output when the file is open.
                            Slave – active output when the power is on.

DSR Data Set Ready: Input signal to check whether the other unit is ready or not.

RTS Request To Send: Output signal to request transmission.

CTS Clear To Send: Input signal to permit transmission.

● Communication Method

Half Duplex Start-Stop Synchronization (See pages 39 ~ 41 for details.)

1 Start Bit, 8-Bit Data, 1 Stop Bit without Parity

Transfer Rate
　　Booting　　　9600bps
　　Operating　　19200bps

(2) One-Chip CPU (HD63A01V1)

This 8-bit central processing unit (CPU) controlling the system of the disk drive has the serial interface, the parallel port, the mask ROM (4 K bytes), and the RAM (128 bytes). The functions of each terminal will be described later. This CPU functions at mode 6. The lower 8 bits of the data and the address are multiplexed. Fig. 6-3 shows the timing. The lower byte of the address is determined at the falling edge of AS. The read/write operations of the data are performed at the falling edge of E. This IC is made by the CMOS process, so that it consumes less power.

Address Strobe (AS)

Enable (E)

R/W, $A_8 \sim A_{15}$ (SC$_2$) (Port4)

MCU Write $D_0 \sim D_7$, $A_0 \sim A_7$ (Port3)

MCU Read $D_0 \sim D_7$, $A_0 \sim A_7$ (Port3)

Fig. 6-3

— 19 —
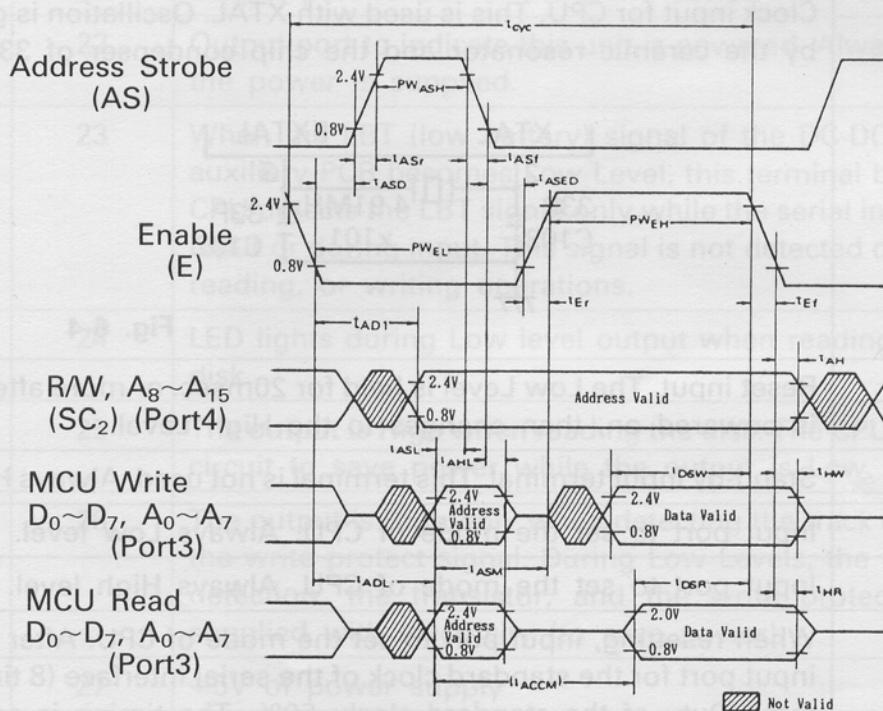
● CPU (HD63A01V1) Terminal and Function

Terminal	Pin No.	Function
$\overline{\text{NMI}}$	4	Non-maskable interrupt input. This unit does not use this terminal. Always High level.
$\overline{\text{IRQ}}$	5	Interrupt input. This unit does not use this terminal. Always High level.
GND	1	Ground
XTAL	2	Clock input for CPU. Oscillation is generated by the ceramic resonator of 4.91MHz and the chip condenser of 33pF.
EXTAL	3	Clock input for CPU. This is used with XTAL. Oscillation is generated by the ceramic resonator and the chip condenser of 33pF. **Fig. 6-4**
$\overline{\text{RES}}$	8	Reset input. The Low Level is held for 20msec. or more after the unit is powered on, then changes to the High Level.
$\overline{\text{STBY}}$	9	Stand-by input terminal. This terminal is not used. Always High level.
P20	11	Input port to set the mode of CPU. Always Low level.
P21	12	Input port to set the mode of CPU. Always High level.
P22	13	When resetting, input port to set the mode of CPU. After resetting, input port for the standard clock of the serial interface (8 times baud rate). Duty of the standard clock: 50%. The timing is as follows. Min 50μsec. **Fig. 6-5**

Terminal	Pin No.	Function
P23	14	Input port to receive the data of the serial interface. High level when there is no communication with the host.
P24	15	Output port to transmit the data of the serial interface. High level when there is no communication with the host.
P10	18	Input port to receive the request to send signal which is the interface control signal from the host.
P11	19	Input port to receive the data terminal ready signal from the host.
P12	20	Output port to permit the transmission from the host.
P13	22	Output port to indicate this unit is powered. Always High level after the power is supplied.
P14	23	When the LBT (low battery) signal of the DC-DC unit through the auxiliary PCB becomes Low Level, this terminal becomes Low. The CPU detects the LBT signal only while the serial interface is awaiting input or during input. This signal is not detected during the seeking, reading, or writing operations.
P15	24	LED lights during Low level output when reading or writing to the disk.
P16	25	The output is High when reading the disk. The CPU stops the reading circuit to save power while the output is Low.
P17	26	The output is High only when detecting the track 0 (zero) signal and the write protect signal. During Low Levels, the LED of the track 0 detection, the transistor, and the write protect switch are not supplied with electricity (to save power).
Vcc	27	+5V of power supply
	6,7,10,16, 17,21,33, 34,38,39, 46~49	These pins are non-connected.

— 21 —

Terminal	Pin No.	Function
P47	28	Address of upper 8 bits.
P46	29	
P45	30	
P44	31	
P43	32	
P42	35	
P41	36	
P40	37	
P37	40	The address of the lower 8 bits and the data of 8 bits are multiplexed. Address/data bus
P36	41	
P35	42	
P34	43	
P33	44	
P32	45	
P31	50	
P30	51	
R/$\overline{\text{W}}$	52	The read/write signal of the CPU. The Low level is output in writing and the High level in reading. The High Level is also output during reset.
$\overline{\text{AS}}$	53	Control signal to separate the address/data bus into the address and the data.
E	54	Output of system clock. The frequency of 4.91MHz is divided one fourth. The RAM and the gate array are accessed when this clock is High. They are written in at the falling edge of this clock.

(3) Gate Array (μPD65002)

The gate array of 857 gates is made through the CMOS process. It consists of the input port, the output port, the dividing circuit, the FM/MFM modulation/demodulation circuit, and the address (lower 8 bits)/data separating circuit. Refer to the following table for functions of each terminal of the gate array.

● Gate Array (μPD65002) Terminals and Functions

Terminal	Pin No.	Function
RD	1	Modulated input signal which is read out of the disk. Pulse width: 250μsec. Pulse interval: approx. 4μsec. or 8μsec.
WE	2	High level output in writing in the disk. The writing circuit functions when WE = High and it does not function when WE = Low to save power.
WD	3	Modulated output data for writing in the disk. The WD is an inverted signal of the WD and vice versa. The width of the High and Low levels is 4μsec. or 8μsec. when writing. And the level is fixed at High or Low when erasing.
WD	4	
AD0	8	Address (lower 8 bits)/data bus. To input or output the multiplexed signals.
AD1	6	
AD2	5	
AD3	52	
AD4	51	
AD5	50	
AD6	49	
AD7	48	
Vcc1	33	+5V Power Supply
Vcc2	7	
A7	9	Address bus (lower 8 bits). The AD0 – AD7 are latched by the AS signal. A0 and A1 are used as signals to select the internal register.
A6	10	
A5	11	
A4	12	
A3	13	
A2	15	
A1	16	
A0	17	
TRK0	18	To input the Low level when the head is at track 0. Therefore, this signal changes from High to Low while the head moves from track 1 to 0. This signal is valid, however, only when the SCAN signal is active (CPU P17 is High level) because the sensor circuit is not supplied with power when SCAN = Low.

— 23 —

Terminal	Pin No.	Function
MTON	19	The DC motor rotates when a High level signal is output. The index signal is valid only when this signal is High. The index circuit stops to save power during Low levels. The rising time of the motor is 1sec.
φ	20	Standard clock input of 8MHz in modulation and demodulation.
COMP0	21	The Low level is input when the battery voltage drops under 3.7V or less. When this signal is input, the PD outputs the High level to turn off the power.
COMP1	22	The Low level is input when the battery voltage drops to 4.0V or less. When this signal is input, battery replacement is required. P15 of the CPU changes to the Low level to indicate "LOW BATTERY".
PD	23	Usually Low level output after power is applied. The power voltage is insufficient, the Low level signal is input to COMP0 and PD outputs the High level to turn off power.
RES	24	The reset input signal. A Low level input makes all functions return to their states: CLOCKOUT = High, PD = Low, WE = Low, and STEP 0 − 3 = High, RES goes High 20msec. or more after power is supplied.
SCLK0	25	Input port to set the operation mode and the baud rate of the serial interface, as follows (the numeral "0 (zero)" indicates the soldered condition on the PCB):
SCLK1	26	
SCLK2	27	
SCLK3	28	

SCLK3	SCLK2	SCLK1	SCLK0		
0	0	0	0	Test Mode 0	9600bps
0	0	0	1		19200bps
0	0	1	0	Test Mode 1	19200bps
0	0	1	1	FDC Mode	150bps
0	1	0	0		300bps
0	1	0	1		600bps
0	1	1	0		1200bps
0	1	1	1		2400bps
1	0	0	0		4800bps
1	0	0	1		9600bps
1	0	1	0		19200bps
1	0	1	1		38400bps
1	1	0	0		76800bps
1	1	0	1	Brother Mode	4800bps
1	1	1	0		9600bps
1	1	1	1		19200bps

Fig. 6-6

Terminal	Pin No.	Function
WPRO	29	Write protect signal input. A High level signal creates a write protect state. Valid only when the SCAN is High because the switch is not supplied with power when Low.
TE STMD	30	Test terminal input to check the gate array. The test mode is set when the TESTMD is at a High level. When the specified signal is input into TEST 0, the information is output from each output terminal to check and test the operations of the circuits.
TEST0	31	
WINDOW	32	Window input terminal in demodulation by MFM. Direct connection with the ground because of FM modulation.
GND	34	Ground
STEP0	35	Output for the excitation of the stepper. Phase excitation is possible when STEP 0 and STEP 2 are in an inverted relationship with STEP 1 and STEP 3 respectively. Refer to the software manual for details on the output state.
STEP1	36	
STEP2	37	
STEP3	38	
MEDIA	39	Input signal to detect whether the disk is set in the unit. A Low level indicates the loading of the disk. The unloading of the disk (the rise of the signal) is detected by the D-FF. The change of the medium is also detected. Detection is performed by the mechanical switches.
INDEX	40	Index signal input. Two types of pulses, a long one and a short one, are input by one rotation. Pulse length: approx. 6 msec. and 3msec.
CS0	42	Input signal to select the register of the gate array. Selects when the CS0 is Low and the CS1 is High.
CS1	41	
CLKOUT	43	Standard clock output of the serial interface to divide the CLKIN $1/2^n$ by the software. The mode of the CPU is set at the High level during reset.
CLKIN	44	Standard clock input of the CLKOUT (1.23MHz). The CLKIN is divided to output the CLKOUT.
E	45	System clock input from the CPU. When this signal is High, the register is accessed.
AS	46	Control signal to separate the address (lower 8 bits) and the data bus.
R/W	47	Signal to read and write in the register. High level in resetting.
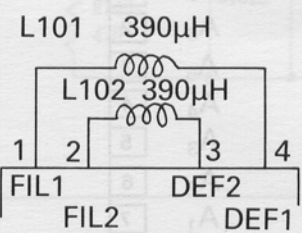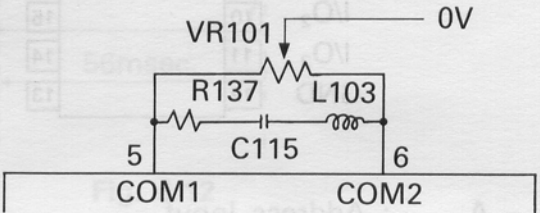
(4) Hybrid IC (MA7339)

This hybrid IC controls the step motor drive and functions even if the power voltage is 3.7V. The control system is supplied with the stabilized power of +5V while the drive system is powered directly by the battery (adapter). The description of each terminal is given below:

Signal	Pin No.	Function
REF	1	Input from the stabilized power supply of +5V
A	2	A-phase control signal input
B	5	B-phase control signal input
C	3	C-phase control signal input
D	6	D-phase control signal input
B−	4	Ground of the power supply
B+	9	Pulse side of the power supply
φA	10	Step motor A-phase output
φB	8	Step motor B-phase output
φC	11	Step motor C-phase output
φD	7	Step motor D-phase output

(5) Hybrid IC (MA7340)

This hybrid IC works for the read/write operations and it may not be supplied with power when not in operation to save power. The descriptions of each terminal are given below:

Signal	Pin No.	Function
FIL1	1	Filter input terminal
FIL2	2	
DEF1	4	
DEF2	3	 Fig. 6-7
COM1	5	Input terminal to adjust the symmetry of circuits. Adjust with the volume.
COM2	6	 Fig. 6-8
RD	7	Read data. Output to generate the pulse of 250nsec. when the magnetic inversion occurs.
GND	8	Ground
Vcc1	12	+5V
Vcc2	10	+12V
WG	9	The WD and WD are written in the disk when the write gate is at the High level. Low level after resetting.
RG	11	Read gate. The RD can output when the read gate is at the High level.
CT	15	Center tap of the head coil
RW1	19	One side of the head coil
RW2	20	Another side of the head coil
CURRENT	16	Input terminal to adjust the current which flows through the head coil when erasing. The current is controlled by the 470 ohm resistor.
WD	17	Input terminal of the write data. The WD is an inversion of WD and vice versa.
$\overline{\text{WD}}$	18	

(6) RAM (µPD449G)

All circuits of the static RAM are made through the CMOS process to achieve power-saving operation.

Connection Diagram (Top View)

A_7 1	24 V_{cc}
A_6 2	23 A_8
A_5 3	22 A_9
A_4 4	21 $\overline{WE}$
A_3 5	20 $\overline{CE_1}$
A_2 6	19 A_{10}
A_1 7	18 $\overline{CE_2}$
A_0 8	17 I/O_8
I/O_1 9	16 I/O_7
I/O_2 10	15 I/O_6
I/O_3 11	14 I/O_5
GND 12	13 I/O_4
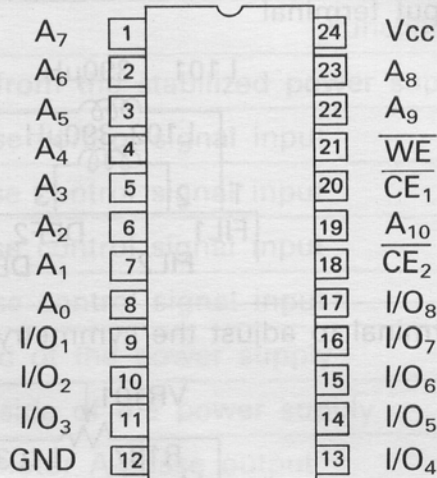
Fig. 6-9. RAM 8320

$A_0 - A_{10}$	: Address Input
$I/O_1 - I/O_8$	: Data Input and Output
CE_1, CE_2	: Chip enable input 1 & 2
WE	: Write enable input
Vcc	: Power source of +5V
GND	: Ground

G. Oscillation Circuit

This oscillation circuit of 8MHz utilizes the condensers of 33P and 68P to equalize the duty.

50H000 1/6   50H000 1/6

Ceramic Resonator 8MHz
68P
C109
1M
R114
x102
C110
33P

Fig. 6-10

— 28 —
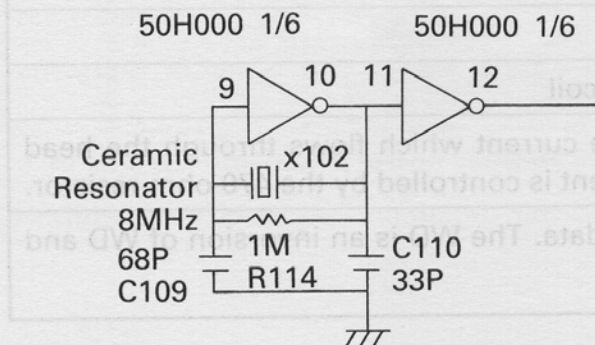
(7) Reset Circuit

Because of the Z104, the Q103 is not turned on unless the power voltage exceeds 4.3V. Therefore, when the power voltage exceeds 4.3V, the power charge starts to the condenser C104.

And when the voltage of the condenser C104 reaches a certain value (after 56msec.), the reset is cancelled.
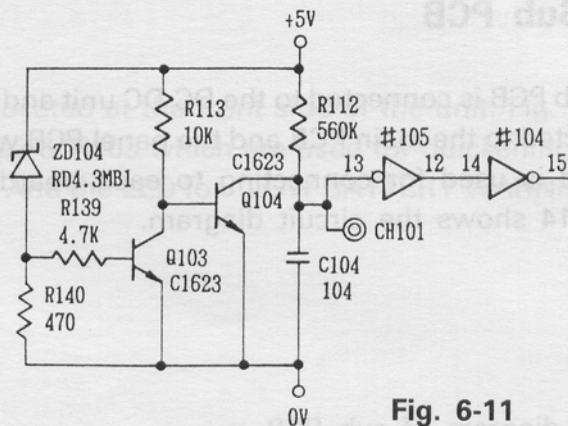
Fig. 6-11
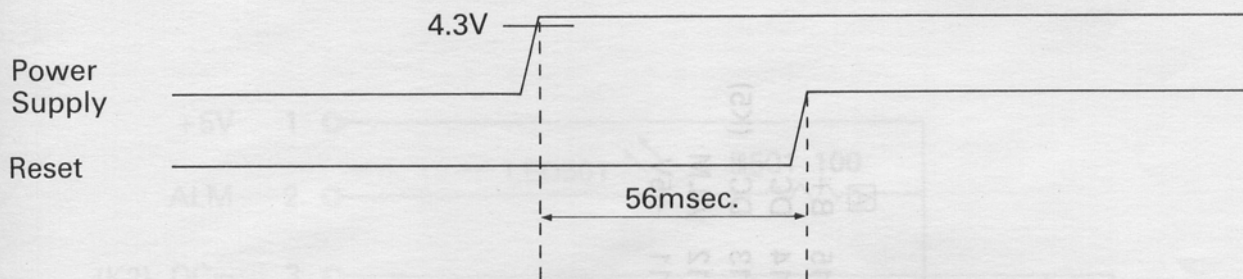
Fig. 6-12

(8) Address Decoder

Fig. 6-13. shows the address decoder. The memory map is as follows:
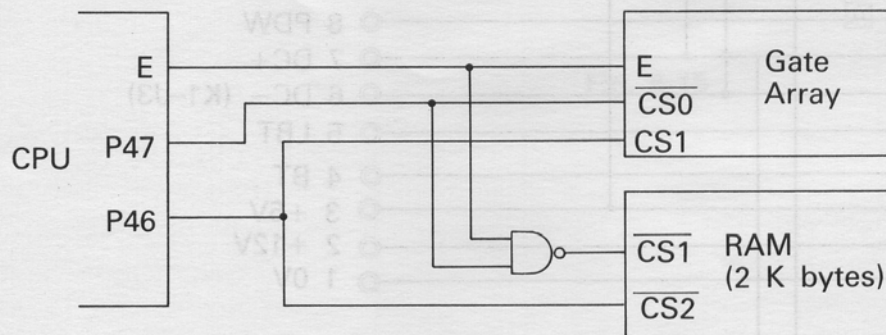
Fig. 6-13

```
00H – 1FH: CPU I/O Port
80H – FFH: CPU Internal RAM (128 bytes)
4000H – 4002H: Gate Array
8000H – 87FFH: RAM (2 K bytes)
F000H – FFFFH: CPU Internal ROM (For 4 K byte Program)
```

6-3. Sub PCB

The sub PCB is connected to the DC-DC unit and the battery (adapter) with the connector and it is connected to the main PCB and the panel PCB with the flat cable. This circuit board has a fuse of 1A and is used for connecting to each board.
Fig. 6-14 shows the circuit diagram.

Circuit diagram of sub PCB.

	J7			9 ALM
PDWN	1			8 PDW
DC−	2			7 DC+
(K4) DC+	3			6 DC− (K1–J3)
LBT	4			5 LBT
EBT	5			4 BT
+5V	6			3 +5V
+12V	7			2 +12V
0V	8			1 0V

Ⓐ F201 1A

Ⓐ 15 B+
14 DC−
13 DC+ (K5)
12 ALM
11 +5V

P9 1 DC+
2 B− (K3)

Fig. 6-14

— 30 —
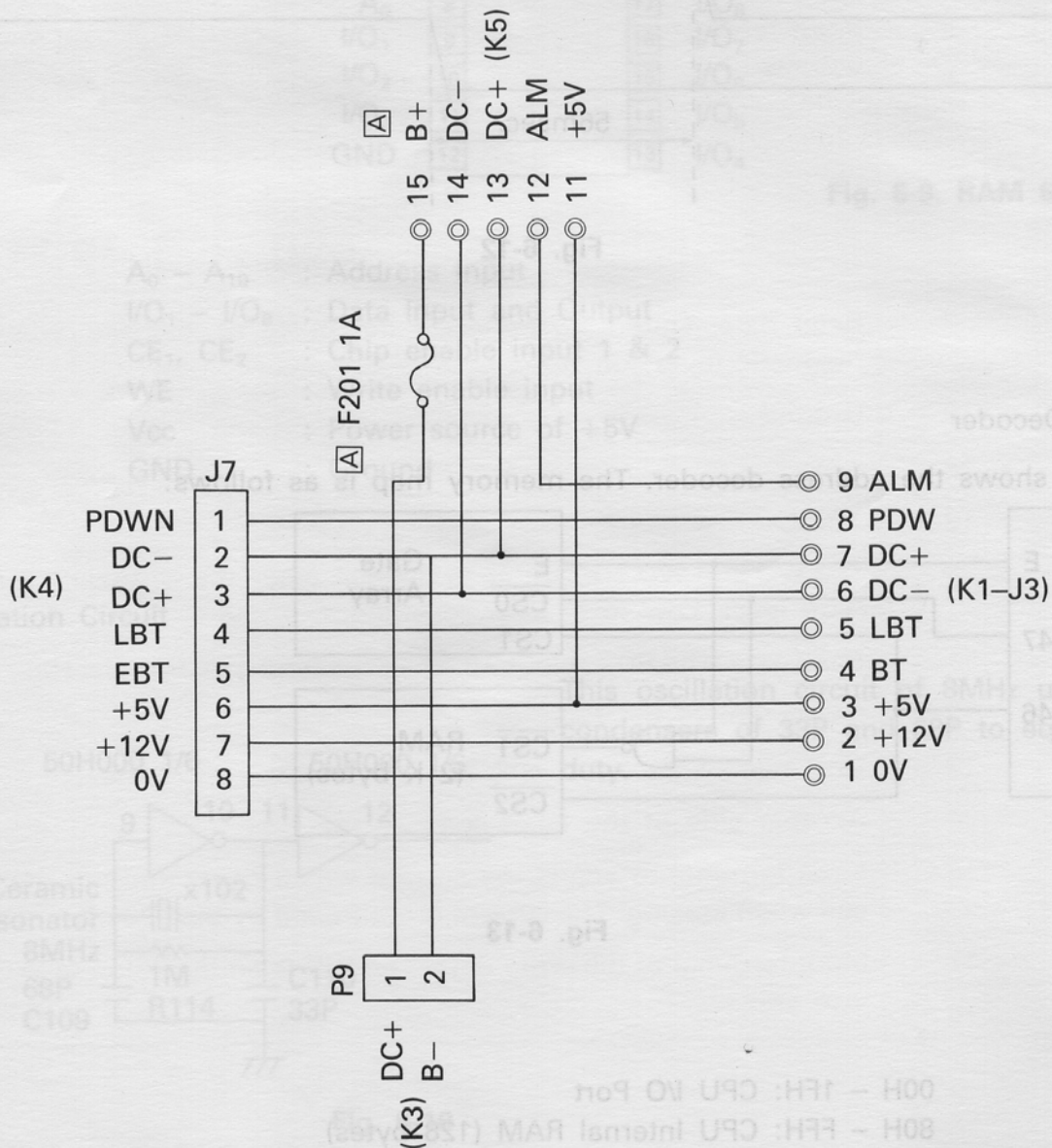
6-4. Panel PCB

The panel PCB is connected to the power switch located at the front side of the unit. Fig. 6-15 shows the twin power switch and the resistors R502 & R503 which are used for quickening the condenser discharge when the switch is turned off. And the LED for "LOW BATTERY WARNING" is lit up by the CPU on the main PCB.

Circuit Diagram of Panel PCB
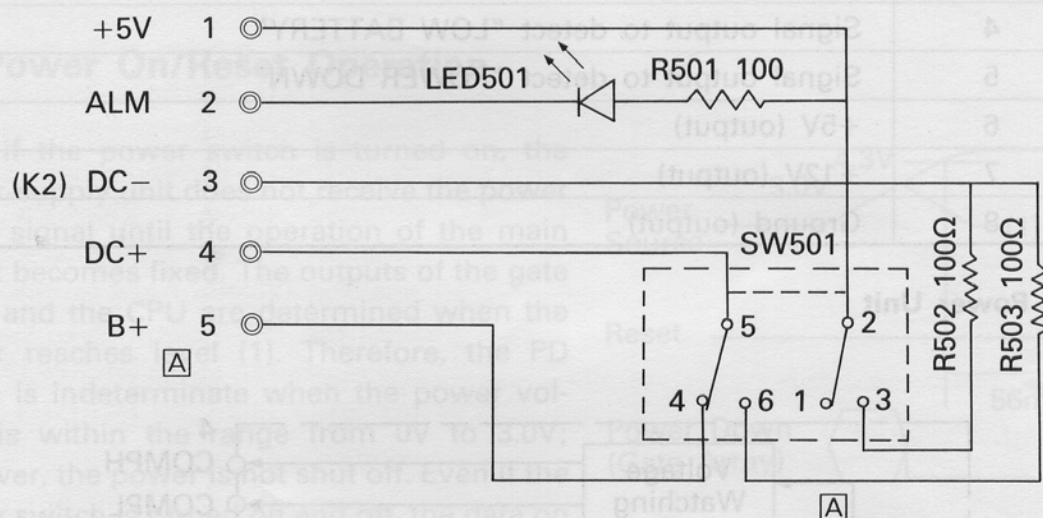
Fig. 6-15

6-5. DC-DC Unit

The DC-DC unit stabilizes the power of +5V and +12V supplied from the battery (or adapter). And it detects the input voltage. When the input voltage is 4.0V or less, the COMPH changes to the Low level. When it is 3.7 or less, the COMPL changes to the low level. When the output is 0V (zero volt) or the power down signal is input, the power is shut off. The descriptions of each terminal follow.

Signal	Pin No.	Function
PDWN	1	Control signal input to shut off the power. Function stops with High level.
GND (IN)	2	Ground (input)
Vcc	3	+ input of battery or adapter: 4 – 10V
COMPH	4	Signal output to detect "LOW BATTERY"
COMPL	5	Signal output to detect "POWER DOWN"
Ch1	6	+5V (output)
Ch2	7	+12V (output)
GND (OUT)	8	Ground (output)

Block Diagram of Power Unit

Fig. 6-16

-32-
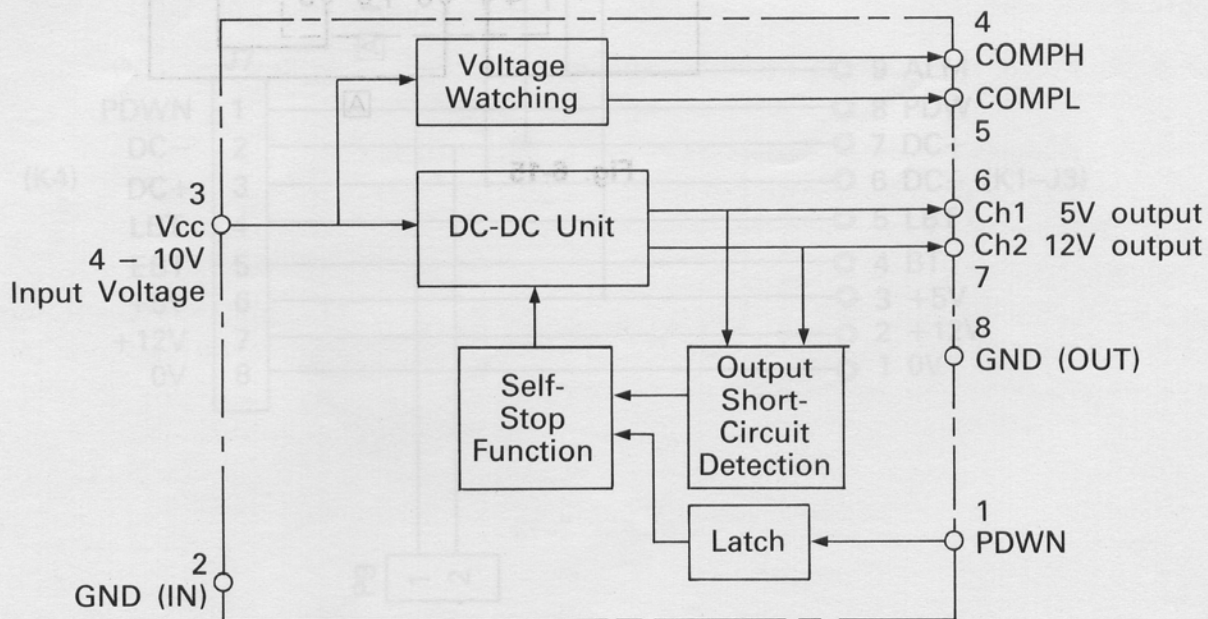
7. EXPLANATION OF BASIC OPERATION

Eight basic operations of this unit are as follows:

1. Power On Reset Operation
2. Track 0 Operation
3. Seek Operation
4. Read Operation
5. Write Operation
6. Interface I/O Operation
7. Power Down & Low Battery Operation
8. DC Motor Drive Operation

Each description will be given in detail on the following pages.

(1) Power On/Reset Operation

Even if the power switch is turned on, the power-supply unit does not receive the power down signal until the operation of the main circuit becomes fixed. The outputs of the gate array and the CPU are determined when the power reaches level (1). Therefore, the PD signal is indeterminate when the power voltage is within the range from 0V to 3.0V; however, the power is not shut off. Even if the power switch is turned on and off, the data on a disk is not disturbed. The write circuit has zener diodes arranged so that it will not work unless the WG signal is 3.5V or more. When the voltage reaches 4.3V, as explained in the
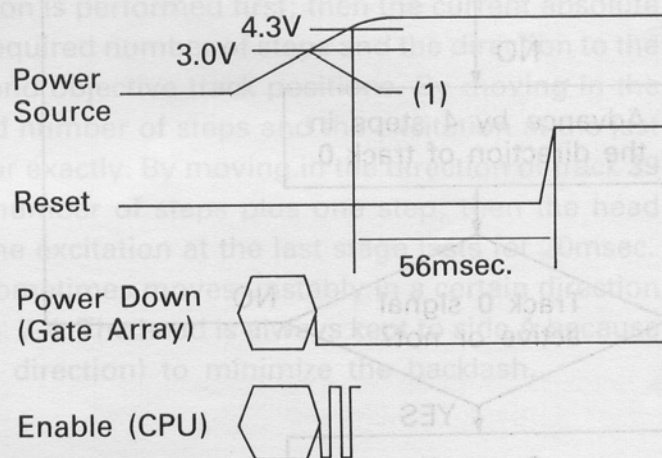
Fig. 7-1

item on the reset circuit, it starts charging the condense; the reset signal changes to the High level 56msec. later. When the reset signal goes High, the CPU determines its operation mode as mode 6, referring to pages 20-23. Then the CPU reads the contents of the internal ROM Addressed FFFEH-FFFFH, and the CPU control shifts to the address set forth by the contents of that location. The gate array sets the internal reset at power on and the initial conditions exist until cancelled by software. These initial conditions are as follows:

Gate Array
PD   Low
WD   Not specified
$\overline{WD}$ Not specified
WE   Low
STEP 0 − 3   High
A0 − A7   Not specified
CLKOUT   High
MTON   Low

(2) Track 0 Operation
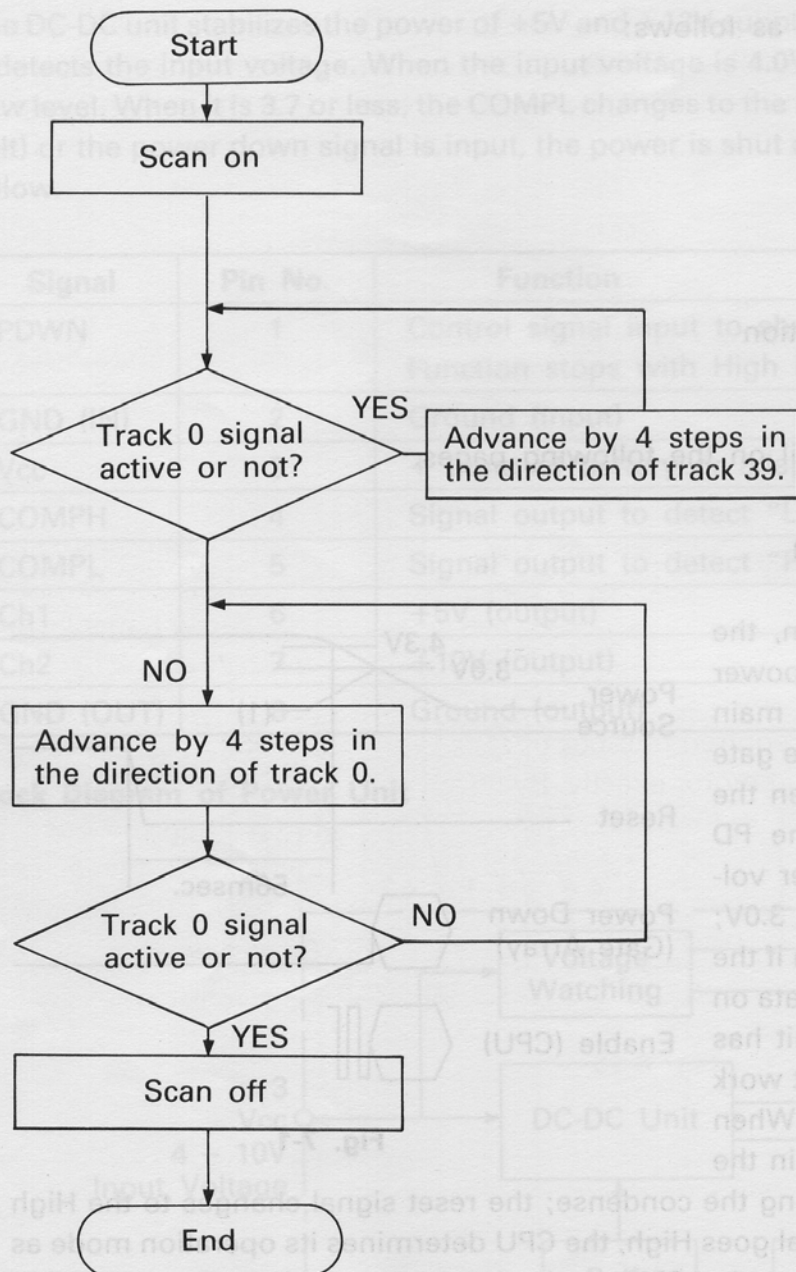
The basic sequence required to move the head to track 0 (zero) is described below. Set P17 of the CPU to the High level at "scan on" and supply the current to the photo-interrupter for sensing the track 0 signal. The track 0 signal varies between the track 0 position and the position where the excitation has the same phase as that of the next track 0 (the position advanced in the direction of the track 39 by 4 steps). If the head is located at position (1), the head is moved until the TRK0 signal changes to High; then it is moved back and stopped when it changes to Low. If the head is located at position (2), the head is moved until the TRK0 changes to Low; the operation stops when P17 of the CPU changes to the Low level.

```
         ┌──────────┐
         │  Start   │
         └────┬─────┘
         ┌────┴─────┐
         │ Scan on  │
         └────┬─────┘
              │
              ▼ ◄──────────────────────────────┐
          ╱─────────╲         YES    ┌──────────────────────┐
         ╱ Track 0    ╲──────────────│ Advance by 4 steps in │
         ╲ signal      ╱             │ the direction of track│
          ╲ active or ╱              │ 39.                    │
           ╲ not?    ╱               └──────────┬─────────────┘
            ╲───────╱                           │
              │ NO                              │
              ▼ ◄──────────────────────────────┘
      ┌──────────────────┐
      │ Advance by 4 steps│
      │ in the direction  │
      │ of track 0.       │
      └────────┬──────────┘
               │
          ╱─────────╲        NO
         ╱ Track 0    ╲─────────────┐
         ╲ signal      ╱            │
          ╲ active or ╱             │
           ╲ not?    ╱              │
            ╲───────╱               │
              │ YES                 │
         ┌────┴─────┐               │
         │ Scan off │               │
         └────┬─────┘               │
         ┌────┴─────┐               │
         │   End    │               │
         └──────────┘               │
```

Track 2   Track 1   Track 0

TRK0

(2)   (1)
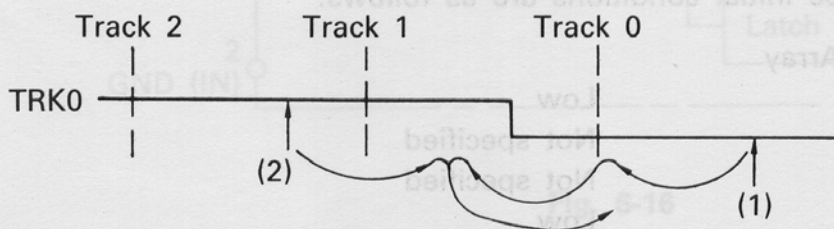
1 Track = 6 Steps

Fig. 7-2

(3) Seek Operation

The operation to move the head between tracks and the method of phase excitation of the stepping motor is explained below. The distance of one track corresponds to six steps of the stepping motor. First the stepping operation will be explained. Fig. 7-3 shows the waveforms of phase excitation of the gate array. There is a difference between the on-off time and the off-on time of transistors. If the switching operation (on & off) is done without regard to this difference, excessive current flows could damage the transistors in an instant. Therefore, all transistors are immediately turned off, then the next phases are excited to prevent damage. This causes a short pulse to appear as shown in Fig. 7-3. The stepping rate is 100PPS. Secondly, the seek operation will be explained; see the flowchart of Fig. 7-5. When power is supplied to this unit, the track 0 operation is performed first; then the current absolute position of the head is memorized in RAM. The required number of steps and the direction to the objective track are calculated from the current and objective track positions. By moving in the direction of track 0, the head moves the required number of steps and the excitation at the last stage lasts for 20msec. to stop the stepping motor exactly. By moving in the direction of track 39 or by zero step, the head moves the required number of steps plus one step; then the head moves in the direction of track 0 by one step. The excitation at the last stage lasts for 20msec. The reason for this movement is that the head sometimes moves unstably in a certain direction because of the head moving mechanism; see Fig. 7-4. The head is always kept to side A because it is moved in one direction (or in the track-0 direction) to minimize the backlash.
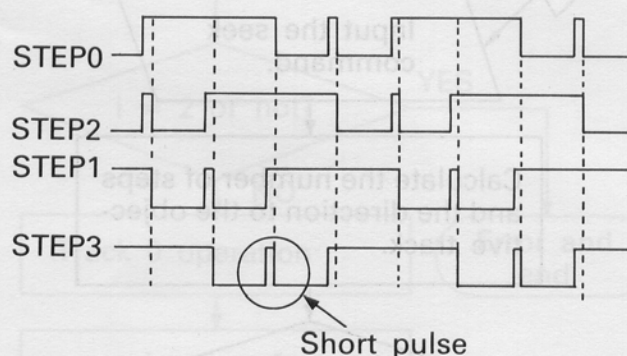
STEP0
STEP2
STEP1
STEP3

Short pulse

Fig. 7-3

Ball to support the head

A
Looseness
Feeding screw

Fig. 7-4

```
        ┌──────────────────────┐
        │        Start         │
        └──────────┬───────────┘
                   │
         ╱─────────▼──────────╲
        ╱  Input the seek      ╲
        ╲  command.            ╱
         ╲────────┬───────────╱
                  │
        ┌─────────▼──────────────────┐
        │ Calculate the number of    │
        │ steps and the direction    │
        │ to the objective track.    │
        └─────────┬──────────────────┘
                  │
              ╱───▼────╲
             ╱ Direction ╲    YES
            ╱  of track 0  ╲──────────┐
            ╲  or not?     ╱          │
             ╲────┬──────╱            │
               NO │                   │
```

The head moves in the direction of track 39 by the required number of steps, plus one. Then it moves in the direction of the track 0 by one step.	The head moves in the direction of track 0 by the required number of steps.

```
        ┌──────────────────────────────┐
        │ The head is excited at that   │
        │ place for 10msec.             │
        └─────────┬────────────────────┘
                  │
        ┌─────────▼────────────┐
        │ Stop excitation.     │
        └─────────┬────────────┘
                  │
        ┌─────────▼────────────┐
        │        End           │
        └──────────────────────┘
```
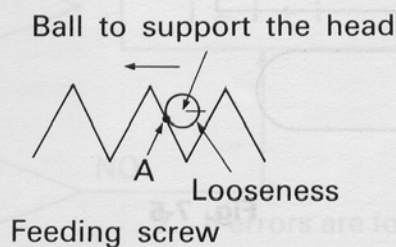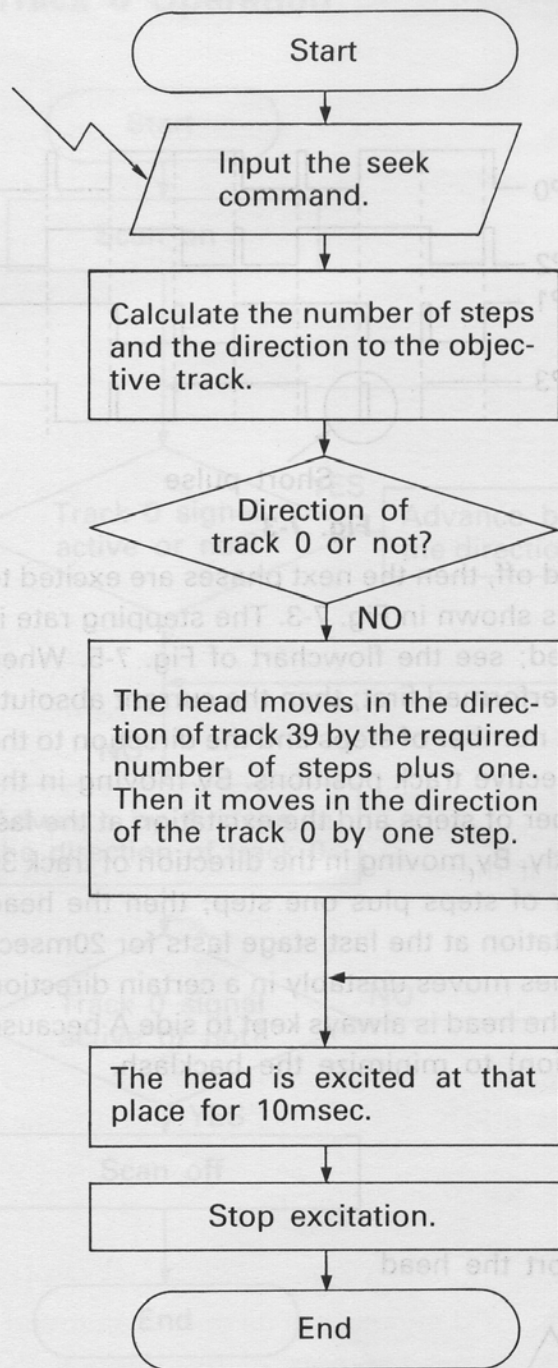
Fig. 7-5

*1) The direction of the head is track 39 when the number of steps is zero. (because the head does not move.)

*2) Direction of Track 0: Outward
Direction of Track 39: Inward

(4) Read Operation

Start

Input the read command.

Does the data of the objective sector exist in the RAM or not? — YES → End

NO

J = 0

i = 0

Seek operation

Read of one hard sector

Read correctly or not? — YES → End

NO

i = 2 or not? — YES → A

NO

A

i = 2 or not? — YES → Error and end

NO

Track 0 operation

j = j + 1

(If errors are found)

i = i + i

When one hard sector is read, the system stores the data into the RAM buffer. If the disk is not changed and the data of the hard sector to be read exists in the RAM buffer, the data is read directly from the RAM buffer but not from the disk; the DC motor does not turn on in this case. If the data does not exist in the RAM buffer, it is read from the disk.

When errors are found in the CRC check, etc., the read operation is retried a maximum of 9 times as follows:

1. The read operation is retried three times at a track where an error was found (target track).

2. If errors are found, the head moves to track 0 and comes back to the target track. The head operation is retried three times.

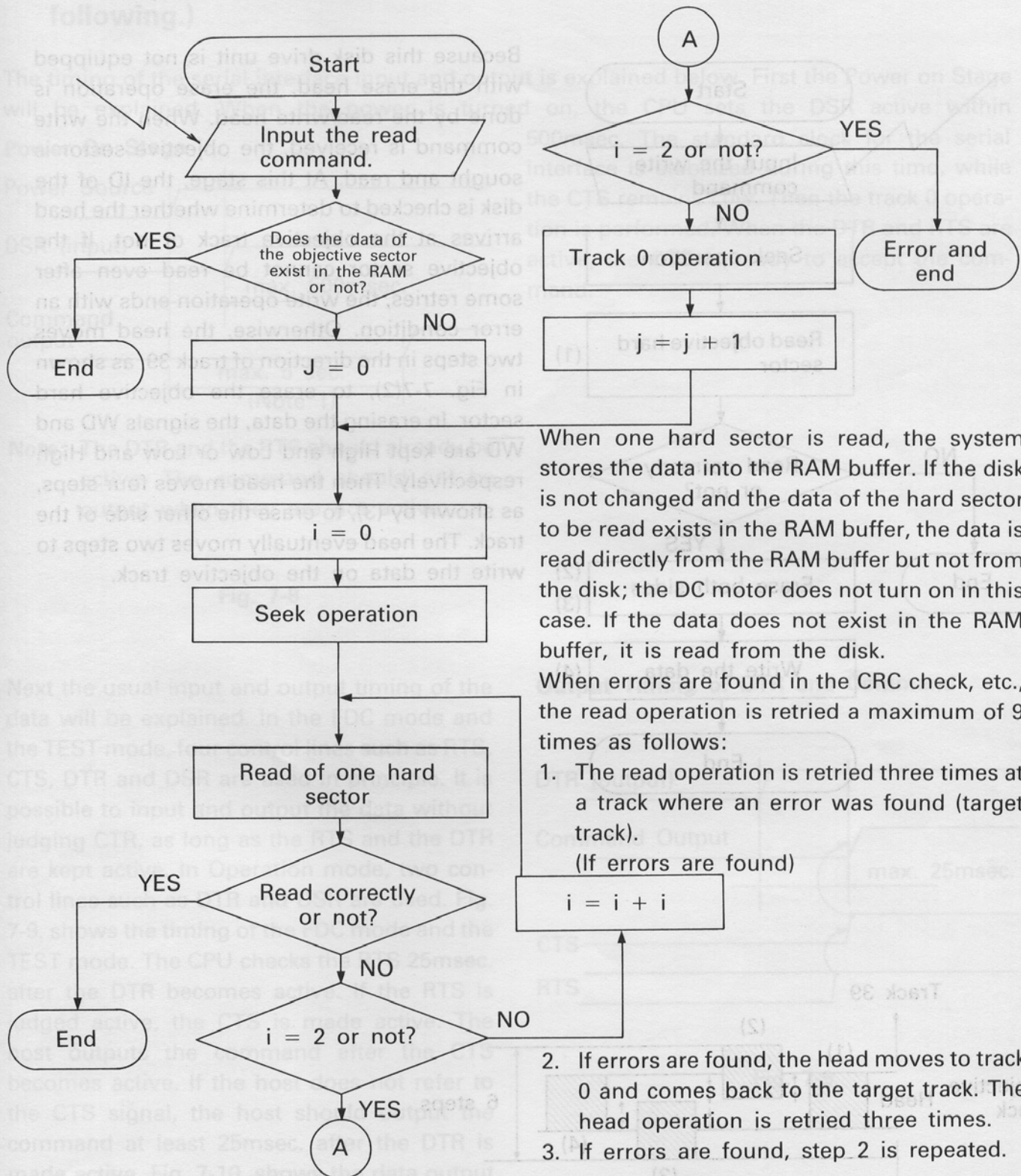3. If errors are found, step 2 is repeated.

Fig. 7-6

When the error cannnot be recovered even after nine retries, the read operation ends in error. The read operation, however, ends immediately (without retries) when the disk is not set or unrecoverable (fatal) errors are found — for example, when the index signal cannot be detected or when the track 0 signal cannnot be detected.
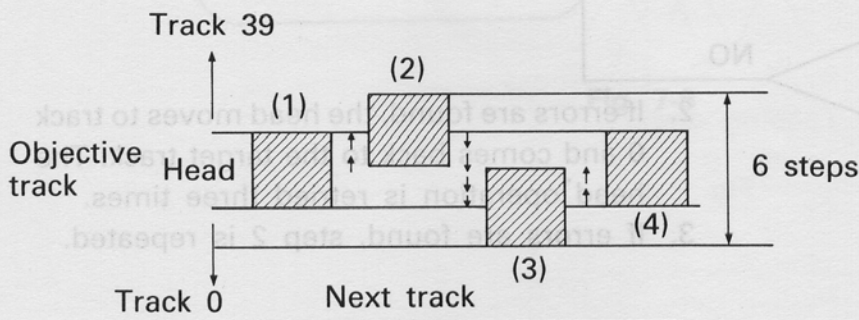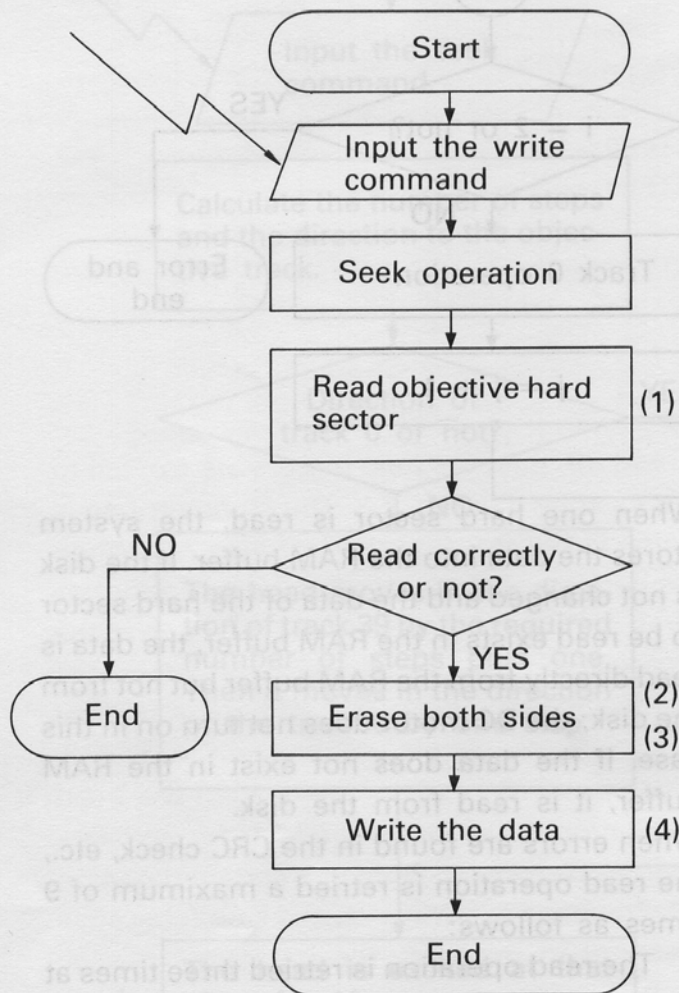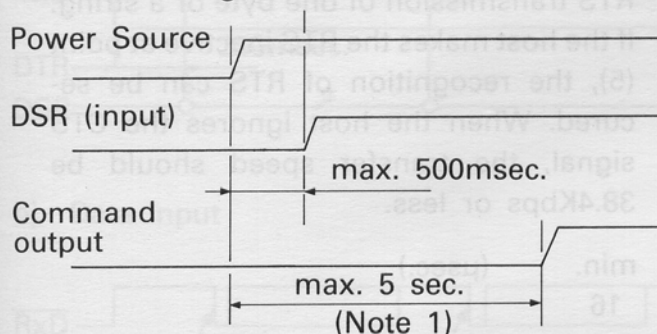
(5) Write Operation

```
                    Start
                      │
                      ▼
              Input the write
                 command
                      │
                      ▼
              Seek operation
                      │
                      ▼
              Read objective hard    (1)
                 sector
                      │
                      ▼
         NO      Read correctly
    ◄────────    or not?
    │                 │ YES
    ▼                 ▼
   End           Erase both sides    (2)
                                     (3)
                      │
                      ▼
                 Write the data      (4)
                      │
                      ▼
                    End
```

Because this disk drive unit is not equipped with the erase head, the erase operation is done by the read/write head. When the write command is received, the objective sector is sought and read. At this stage, the ID of the disk is checked to determine whether the head arrives at the objective track or not. If the objective sector cannot be read even after some retries, the write operation ends with an error condition. Otherwise, the head moves two steps in the direction of track 39, as shown in Fig. 7-7(2), to erase the objective hard sector. In erasing the data, the signals WD and $\overline{WD}$ are kept High and Low or Low and High respectively. Then the head moves four steps, as shown by (3), to erase the other side of the track. The head eventually moves two steps to write the data on the objective track.

```
  Track 39
     ↑
     │          (2)
     │    (1)   ▨
 Objective ▨    ▨        ▨
 track   Head  ↕    (3)  ↕      6 steps
     │         ▨    ▨    (4)
     │              ▨
     ↓          (3)
  Track 0    Next track
```

Fig. 7-7

(6) Interface I/O Operation (The signal names of the host are used in the following.)

The timing of the serial interface input and output is explained below. First the Power on Stage will be explained. When the power is turned on, the CPU sets the DSR active within 500msec. The standard clock for the serial interface is stabilized during this time, while the CTS remains Low. Then the track 0 operation is performed. When the DTR and RTS are active, the CTS is ready to accept the command.

Power On Stage

Power Source

DSR (input)

max. 500msec.

Command output

max. 5 sec.
(Note 1)

Note: The DTR and the RTS should already be active. The command should not be output when they are not active.

Fig. 7-8

Next the usual input and output timing of the data will be explained. In the FDC mode and the TEST mode, four control lines such as RTS, CTS, DTR and DSR are used in principle. It is possible to input and output the data without judging CTR, as long as the RTS and the DTR are kept active. In Operation mode, two control lines such as DTR and DSR are used. Fig. 7-9. shows the timing of the FDC mode and the TEST mode. The CPU checks the RTS 25msec. after the DTR becomes active. If the RTS is judged active, the CTS is made active. The host outputs the command after the CTS becomes active. If the host does not refer to the CTS signal, the host should output the command at least 25msec. after the DTR is made active. Fig. 7-10. shows the data output

Output Timing of DTR and Command

DTR (output)

Command Output

max. 25msec.

CTS

RTS

Fig. 7-9

operation. The DTR and the DSR are in the active condition. When the RTS becomes active, the Portable disk drive detects it and make the CTS active.
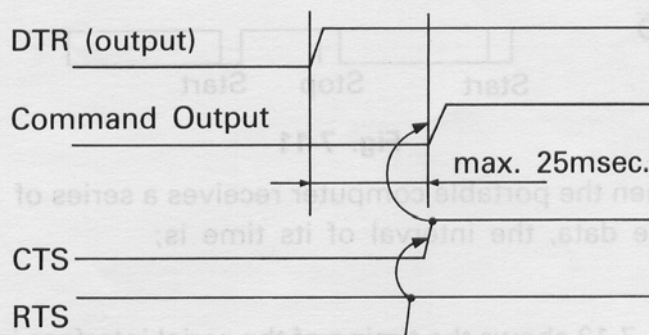
(1) After the host finds the CTS to be active, it outputs the serial data.

- 39 -

Data Output
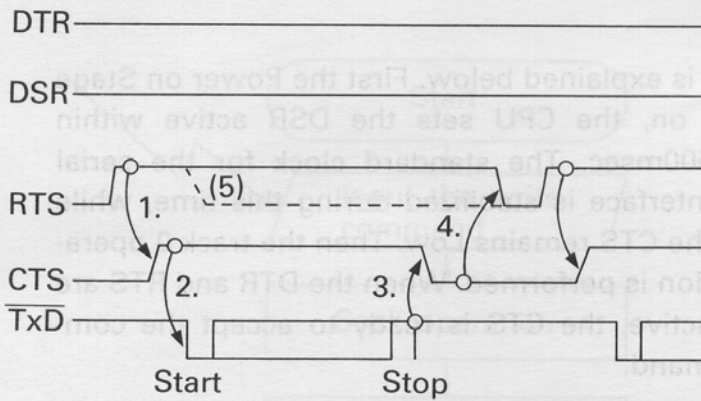
Fig. 7-10

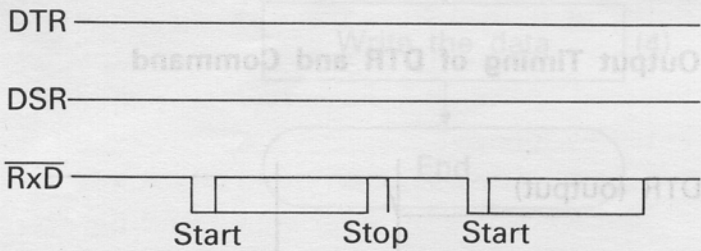|	max.	min.	(µsec.)
CTS is asserted after RTS is asserted.	110	16	
CTS is negated after data is output (after the stop bit is output.)	140	42	
RTS is checked after CTS is negated.		28	

Data Input

Fig. 7-11

When the portable computer receives a series of byte data, the interval of its time is;

max.	min.	(µsec.)
125	30	

Fig. 7-12 shows the timing of the serial interface in Operation mode. After the host finds the DSR to be active, it outputs the data. The maximum speed of transmission is 19200bps. It takes 200msec. for the host to make the TxD line stable after the DTR becomes active; the host outputs the data 200msec. later.

(2) Portable disk drive receives the serial data to make the CTS active.

(3) Then, after the host finds the CTS to be inactive, it makes the RTS inactive. Because the portable disk drive does not check the RTS line, the host may make the RTS transmission of one byte or a string. If the host makes the RTS inactive at point (5), the recognition of RTS can be secured. When the host ignores the CTS signal, the transfer speed should be 38.4Kbps or less.

The data input operation will be explained next. When the DTR is active, the portable disk drive decides which data can be output and outputs it. The start bit of the following byte should be input into the host within a maximum of 30 sec. after the stop bit of the preceding byte is input. Therefore, the data should be input less than every
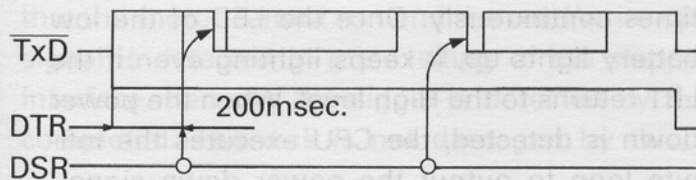
$$30 + \frac{1,000,000}{\text{baud rate (bps)}} \text{ [µsec.]}.$$

Serial Interface Timing
(Operation Mode)
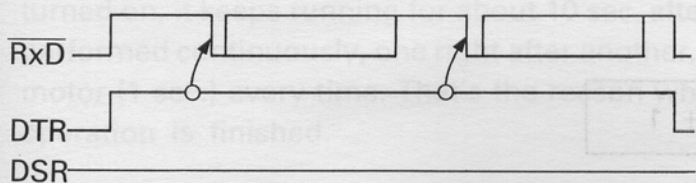
a) Data Output

b) Data Input

Fig. 7-12

In inputting the data, the CPU outputs the data after it confirms that the DTR is active. The maximum speed of transmission is 9600bps; therefore, the data is communicated at a speed of 9600bps with regard to the Portable Disk Drive.

This unit can be set in the initial reset condition by using communication lines. However, this software reset can be used only in the FDC and TEST modes. The first method: When the DTR is inactive for at least 500msec., the portable disk drive decides the host is down, and returns to the initial state of the command input queue to cancel the command already input. The second method: Because the CPU recognizes the command and the data in a string, the Portable disk drive decides the host is down if the strings are suspended for at least 5 sec. or more.
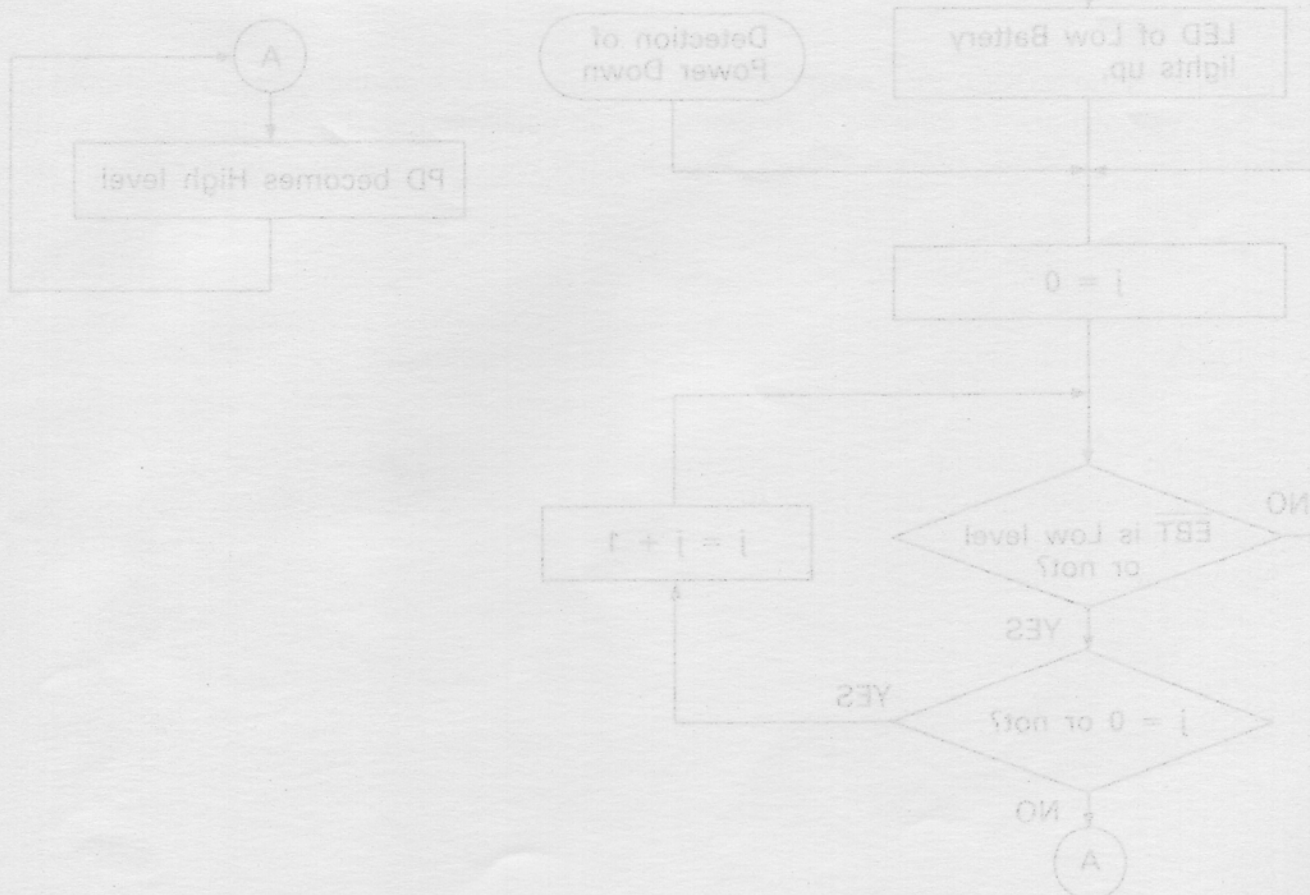
(7) Power Down and Low Battery Operation

As shown in the following flowchart, the power down signal and the low battery signal are output only when they are detected two times continuously. Once the LED of the low battery lights up, it keeps lighting even if the LBT returns to the High level. When the power down is detected, the CPU executes the infinite loop to output the power down signal.

Detection of Low Battery

i = 0

$\overline{\text{LBT}}$ is Low level or not? — NO / YES

i = i + 1

i = 0 or not? — YES / NO

LED of Low Battery lights up.

Detection of Power Down

A

PD becomes High level

j = 0

$\overline{\text{EBT}}$ is Low level or not? — NO / YES

j = j + 1
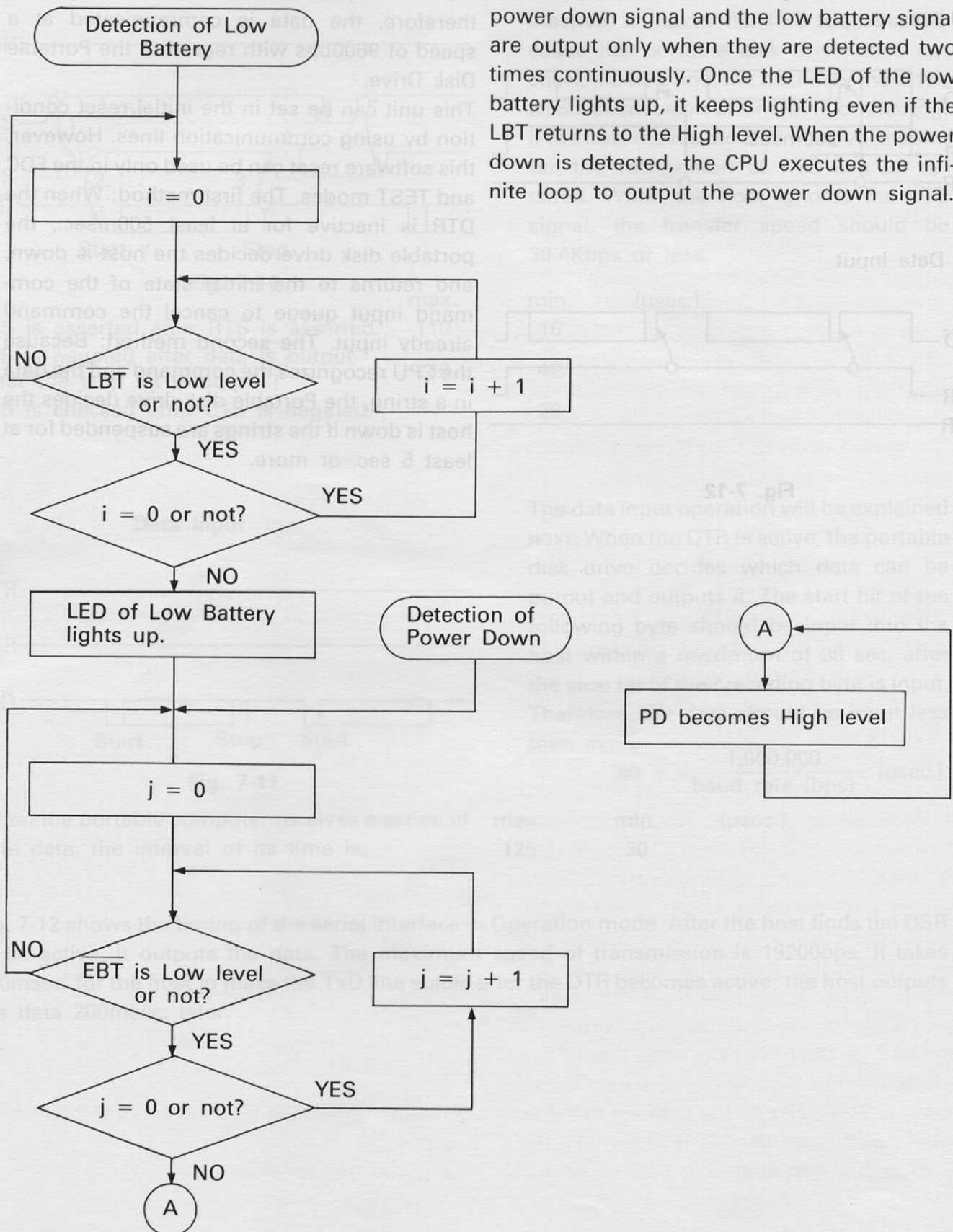
j = 0 or not? — YES / NO

A

Fig. 7-13

Even if the low battery signal (LBT) becomes active, the power remains in the battery to do the formatting several times, so that the current operation (for example, read or write operation) can be completed. Therefore, the low battery is detected only in the serial interface queuing state (waiting for the command or the data input from the host).

When the battery voltage is lowered to this extent, the unit goes into the power down state, so that the motor cannot run and the read/write operations cannot be performed. The power down signal is detected in the exciting of the stepper, rising the DC motor, and queuing the serial interface. Because the signal is detected by the software, the current operation might not be completed. The disk is not damaged by this, however.

(8) DC Motor Drive Operation

The DC motor is turned on when the read/write operations are actually performed. Once it is turned on, it keeps running for about 10 sec. after the operation is finished. When operations are performed continuously, one right after another, there is no need to wait for the rising time of the motor (1 sec.) every time. That's the reason why the motor keeps running for 10 sec. after one operation is finished.

8. STANDARD MAINTENANCE

8-1. Exerciser Portable Computer and Adjusting Tools

(1) Necessary Apparatus

    a. MODEL 100/TANDY 200
    b. CE (alignment) disk
    c. Oscilloscope (2 channels)
    d. Various types of drivers
    e. Soldering iron and solder
    f. Normal disk
    g. Counter

(2) Checkpoint of Main PCB (See Fig. 10-1 on page 56.)

Point on the main PCB

1) CH102 or CH103 .... Wave from output signal of
                                                  read/write head
2) CH120 .... Index signal
3) CH121 .... Track 00 signal
4) 0V .... Ground
5) Switch Part

When using the MODEL 100/TANDY 200, the dip switch of the portable disk drive should be in the ON position. To observe each signal on an oscilloscope, the ground of the probe should be 0V and the probes should be connected with the checkpoints of each signal.
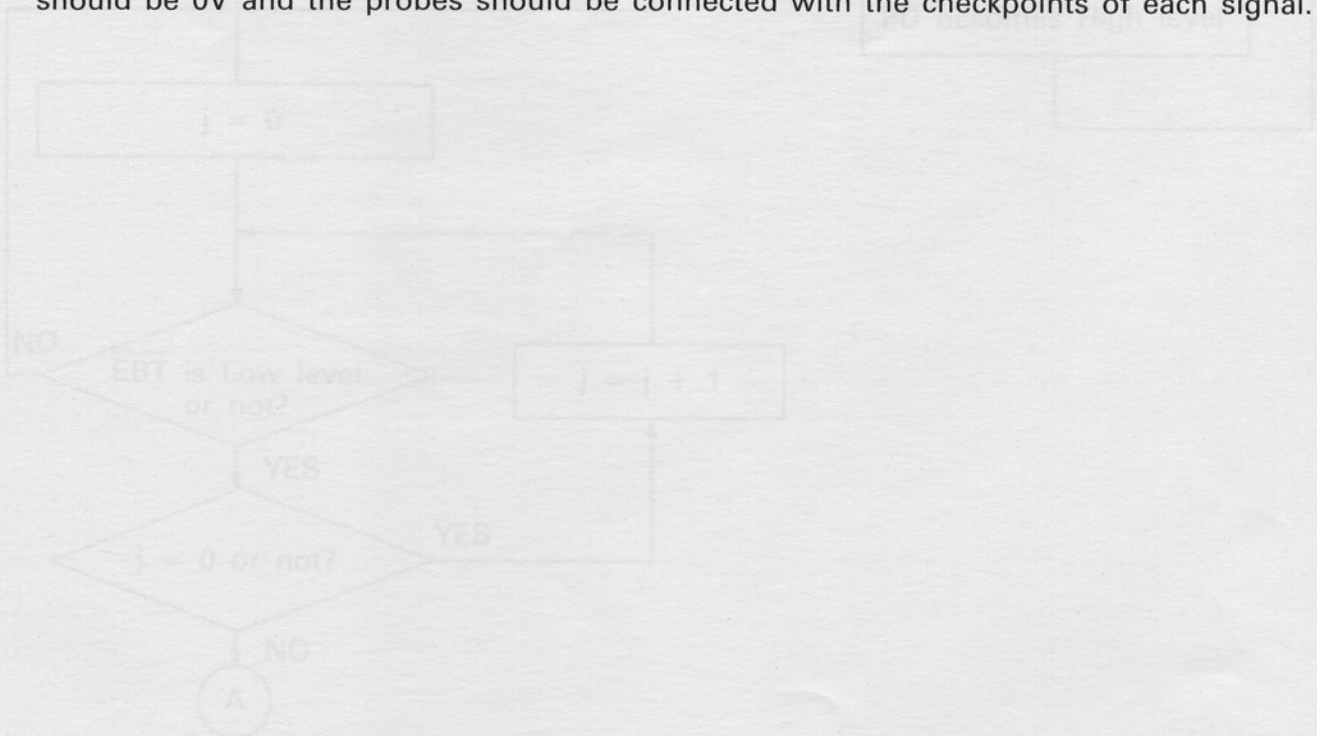
(3) Operation of MODEL 100/TANDY 200

1. Check to be sure that the dip switches are all in the ON position.
2. Connect the portable disk drive to the MODEL 100/TANDY 200 with the cable.
3. Turn on the power switch of the MODEL 100/TANDY 200.
4. a. Set the MODEL 100/TANDY 200 in menu mode.
   b. When the menu is not on the screen, press the F8 key after pressing the shift key and the break key simultaneously.
      The menu appears on the screen by these key operations.
      (Program stops by depressing the shift key and the break key simultaneously.)
5. Load the "MICTDC" program from the alignment tape (Part No. AXX-2049 for 26-3808). For instructions on loading this program, refer to the manual included with this tape.
6. Select "MICTDC" with the cursor and press ENTER. Then "Reset Drive, wait 3 sec. and press ENTER" appears on the screen.
7. After turning off the power switch of the portable disk drive, turn on the power again. At this time, check that the stepping motor runs and the head is moved to track 00. If the stepping motor does not run, the PCB and/or the stepping motor must be defective.
8. Wait approx. 3 sec. after the drive is reset, then press any key to start the test. The message "Loading Driver into Drive" will be displayed, followed by "Initiating Drive". Then the menu should be displayed. If not, break the program and try it once more. Remember to reset the drive after the program has begun, wait 3 sec. and press ENTER. If the menu doesn't come up, and the low power light of the drive blinks, then there may be a problem in the drive.
9. Below is a sample Menu screen:

```
TDC–Tandy Portable Drive        00/00/00
Track = 0            Error = 0           Offset = 0
0 = Track-0          1 = Speed Check     2 = Carriage
3 = Head Amp         4 = head Radial     5 = Raw Data
6 = TRK-0 AJ         F = Format DRV      S = Seq Test
Q = Quit             ←→ = Step TRK       ↑↓ = STP Elastic
Select Test = >
```

10. Press the key corresponding to each command.

Key	Command Name	Comments
0	Track-0	Move head to track-0
1	Speed Check	Display Drive Speed
2	Carriage Test	Step between TK-0 & TK-39
3	Head Amplitude	Step to TK-39 for HA Test
4	Head Radial	Head Radial/Azimuth test
5	Raw Data Test	Write 1F or 2F to TK-39
6	Track 0 Adjustment	Step to track-0 for TK-0 sensor Adj
F	Format Drive	Format all 40 tracks on drive
S	Sequential Test	Sequential Read or Read/Write
Q	Quit	Exit Program
←	Step In	Step to next higher track
→	Step Out	Step to next lower track
↑	Step Out Elastic	Step to TK-0 and back to original track
↓	Step In Elastic	Step to TK-39 and back to original track

Notes:

1. 1F = 62.5 KHz   2F = 125 KHz
2. When checking the drive speed, it should be between 298.5 and 300 RPM. The encoder has two notches. If one of the notches of the encoder is covered up, the rotational speed displayed by this test program will be half the actual speed.
3. The Format command can only be stopped by turning off the drive.
4. The Sequential test requires that the diskette has already been formatted by using the FORMAT: command.
5. The drive must be reset every time the program is rerun.

Entry	Contents	Input Parameter
415	Track 0	
500	Read HS	HS: Hard sector No. (0 − 79)
		OS: Degree of offset
		(−128 − +127)
600	Write HS	HS/OS: Same as Read HS
		WD: Write data (0 − 255)
700	Seek	Same as Read HS
800	1F/2F Write	FM: 0 − 1F
		255 − 2F
900	Index burst	
1000	Motor ON/OFF	MT: 0 − OFF, others − ON
1050	Sensor ON/OFF	SE: 0 − OFF, others − ON
1100	Read Gate ON/OFF	RG: 0 − OFF, others − ON
1200	Format	

Notes:

1. HS = Hard Sector.
2. OS = Stepper Offset. Offset range = ⁻128 to ⁺127. 0 = No Offset.

12. Error Code

Error Code (Hex)	Error Code (Decimal)	Contents
10	16	Error in parameter assignment
11	17	
12	18	Logical sector parameter error
13	19	Hard sector No. parameter error
14	20	
20	32	Overflow of parameter values
21	33	Assignment of parameter characters other than '0' – '9'
22	34	Assignment of parameter characters other than '0' – 'F'
30 ≀ 3F	48 ≀ 63	Improper assigned value of parameter corresponding to each command
A0	160	CRC check error in ID section in reading
A1	161	CRC check error in DATA section in reading
A2	162	Seek error in reading
A4	164	IN trigger or no start mark
A5	165	Hard sector length error in reading
B0	176	Write protect
C0	192	Command buffer overflow
C1	193	Command name error
D0	208	Receive error
D1	209	Disk ON error
D3	211	Change disk error
E0 ≀ E2	224 ≀ 226	Host down
F0	240	Without index signal
F1	241	Without track 0 signal
F2	242	Incorrect index signal width

(4) Adjustment with MODEL 100/TANDY 200

Put tape which is impervious to light over the smaller cut of the encoder.
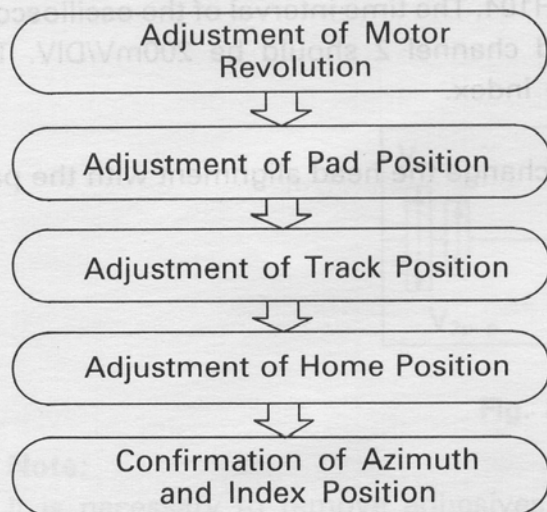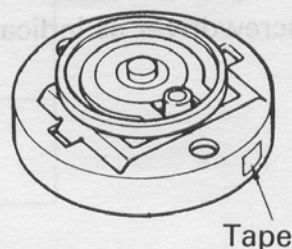

Flowchart of Adjustment

Tape

Fig. 8-2

1. Check to be sure that the screen returns to the condition shown in the subsection (3)-8.
2. Use a normal formatted disk.
3. Perform the running operation.
   - Press the 2 key of the MODEL 100/TANDY 200 to perform the Carriage test. The drive should step continuously between track-0 and track-39. Check for proper movement of the stepper motor. Press the ⟨ESC⟩ key to return to the menu.
     Note:
     The error "160" − "165" might be found.
     This error is not an abnormal condition.
     You can go on to the next step.
4. Adjust the speed.
   - Press 1 to select the speed test. The computer shows half the actual speed because of the tape on one of the Revolution Encoders. The Frequency counter will show the correct speed.
   - Connect the ground of the probe of the counter to the 0V shown in Fig. 10-1. and the probe to the index signal of the CH120.
   - Insert a screwdriver into the part of the DC motor indicated by the arrow in Fig. 8-3. Turn the screwdriver so that the value of the counter is within the range from 4.975Hz to 5Hz. Attach the cover after making the adjustment. Press ⟨ESC⟩ to exit to the menu.
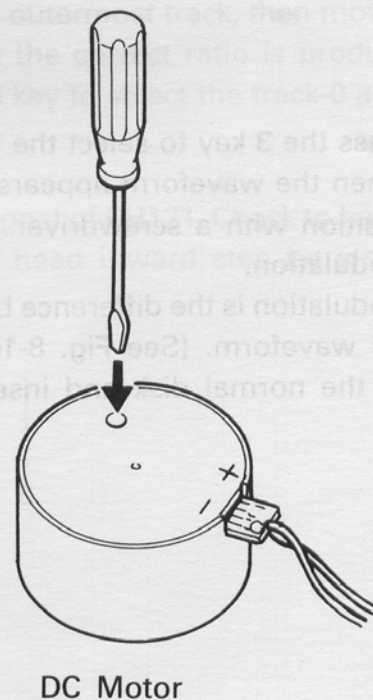

DC Motor

Fig. 8-3

5. Connect the ground lead of the channel 1 probe of the oscilloscope to the 0V shown in Fig. 10-2. Connect the probe to the index signal of CH120. Connect the channel 2 probe of the oscilloscope to the waveform output of CH103 or CH104. The time interval of the oscilloscope is 20msec./DIV. Channel 1 should be 1V/DIV and channel 2 should be 200mV/DIV. The triggering is done at channel 1 according to the index.

6. Adjust the pad position.
   ● Insert the screwdriver as indicated in Fig. 8-4 to change the head alignment with the pad.
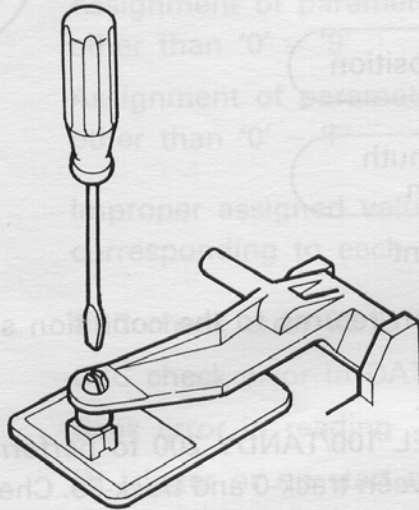
Fig. 8-4. Pad Arm Assembly

   ● Press the 3 key to select the Head Amplitude test. This will write a 2F pattern to track-39. When the waveform appears on the oscilloscope, as shown in Fig. 8-4-1, adjust the pad position with a screwdriver for the greatest signal amplitude with the least amount of modulation.
   Modulation is the difference between a maximum amplitude and a minimum amplitude on the waveform. (See Fig. 8-10.) Press the ESC key to return to the menu.

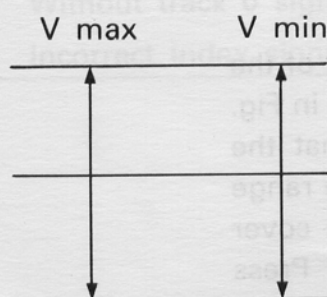7. Eject the normal disk and insert the CE (alignment) disk.

V max   V min

Fig. 8-4-1. Head Amplitude

8. Adjust the track position.
   - After moving the head to track 20 where a digital cat's eye is recorded, turn the stepping motor for the head feed by hand so that two outputs just after the index are almost equal to each other ($V_{1p-p} = V_{2p-p}$), as shown in Fig. 8-5.
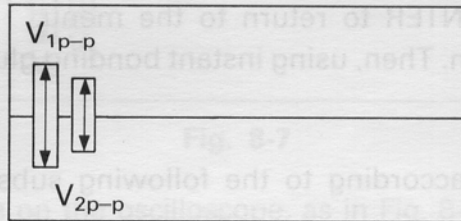

Fig. 8-5. Cat's Eye

Note:
It is necessary to remove adhesives for readjustment because the adjusted stepping motor is glued.

   - Press the 4 key to select the Head Radial test; then set channel 2 of the scope to 100 mv/div. The waveform appears on the oscilloscope as in Fig. 8-5. Check to see if the ratio of V_{2p-p} to V_{1p-p} is within the range from 0.925 to 1.075. If not, turn the stepping motor little by little by hand so that the V_{1p-p} is almost equal to the V_{2p-p}. Press the up arrow key for an elastic step in, the down arrow key for an elastic step out and check the ratio of the signal again. An elastic step moves the head to the innermost or outermost track, then moves it back to its original position. Repeat this procedure until the correct ratio is produced. Press the ESC key to return to the menu; then press the 6 key to select the track-0 adjust test.

9. Adjust the home position (Track 00).
   - Connect the channel 1 probe of the scope to the track 00 signal of CH121. Check to be sure that the signal is about 0V (zero volt). Then move the head inward step by step.
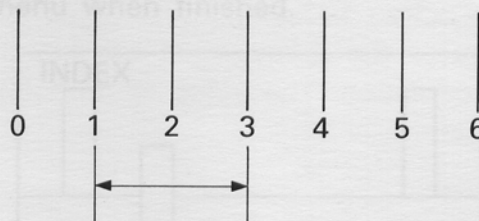

Fig. 8-6

Adjust the photo-interrupter signal to toggle from about 0V to 5V while the head moves between the −1 step and −3 step.

- Once executing the Track-0 Adjust test, enter "−1" (negative 1) for an offset. The track-0 should be about 0V. If it is about 5V, then move the photo-interrupter a little inward. Then press the 0 key and repeat the above-mentioned procedure.
- Now enter "−3". The track-0 signal should change to about 5V. If it is about 0V, then move the photo interrupter a little outward. Enter "0" and repeat the procedure from the beginning. Press E then ENTER to return to the menu.

10. Repeat procedure 9 once again. Then, using instant bonding glue, glue the photo-interrupter to the chassis.
11. Complete the adjustment.
12. Be sure to inspect the unit according to the following subsection (5).

(5) Inspection with MODEL 100/TANDY 200

Inspection with MODEL 100/TANDY 200 is necessary for checking whether the portable disk drive is properly adjusted in accordance with subsection (4).

1. Connect the ground lead of the channel 1 probe of the oscilloscope to the 0V, and the probe to CH120. Connect the probe of the oscilloscope to CH102 or CH103.
   Connect the ground lead of the frequency counter probe to the 0V shown in Fig. 10-2, and the probe to the index signal of CH120.
2. Check to be sure that the screen is like the one shown in subsection (3)-8. Then insert the CE disk.
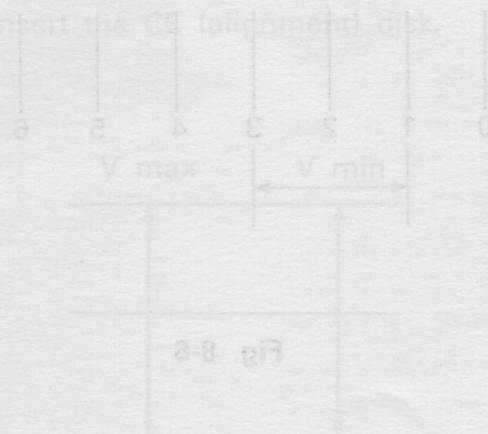
3. Press the 4 key to select the Head Radial test.
   Measure the output of the digital cat's eye.
   The ratio of V_{2p-p} to V_{1p-p} is within the range from 0.80 to 1.20.
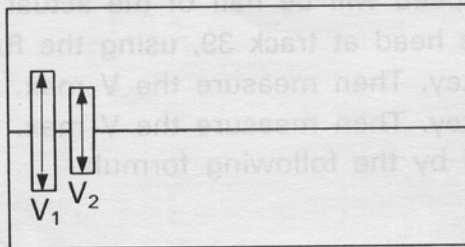
Fig. 8-7

When the waveform appears on the oscilloscope, as in Fig. 8-7., measure the first V1 and V2.

4. To look at the Head Azimuth, press ENTER while running the Head Amplitude test.
   Measure the azimuth. (Set the azimuth within $\pm15'$) Press ⟨ESC⟩ when finished to return to the menu.
   - $\pm0'$ when $V3 = V6 < V4 = V5$
   - $+15'$ when $V6 < V3 = V4 < V5$
   - $-15'$ when $V3 < V5 = V6 < V4$
   Therefore,
   - $\pm15'$ when $V3 \leqq V4$ and $V5 \geqq V6$
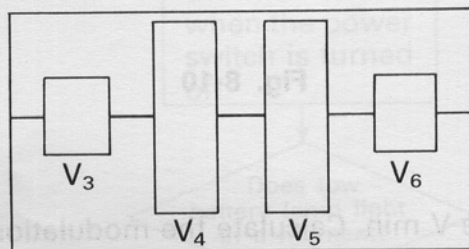
Fig. 8-8

5. Go to track-0 to measure the index position. (within $5 \pm 1ms$)
   This can be done by pressing the 6 key to select the track-0 adjust test, and by entering an offset of 0. This positions the head over the index burst signal.
   Press E to return to the menu when finished.

Fig. 8-9

6. Eject the alignment disk, remove the tape covering one of the revolution decoders, and insert a normal disk. Press the 1 key to select Speed test, and make sure the speed is between 298.5 and 300 RPM. Press ESC when finished. If the tape was left covering one of the encoders, the displayed speed will be half of the actual speed.

7. Measure the resolution of the head at track 39, using the RAM DATA test (#4).
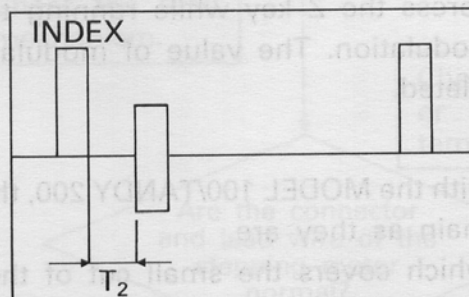   - Write the 1F; press the 1 key. Then measure the V max. shown in Fig. 8-10 (V_{1F}).
   - Write the 2F; press the 2 key. Then measure the V max. shown in Fig. 8-10 (V_{2F}).
   - The resolution is calculated by the following formula.

$$\frac{V2F}{V1F} \times 100\% \text{ (The output of 2F should be more than 300mV.)}$$

   - The resolution must be more than 60%.
   Measure the modulation.
   - Write 2F data on a disk; then the waveform appears on the oscilloscope like below.
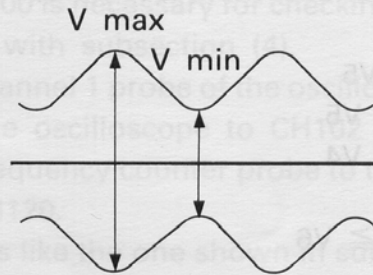
Fig. 8-10

   Measure the V max. and the V min. Calculate the modulation by the following formula.

$$\frac{V \text{ max.} - V \text{ min.}}{V \text{ max.} + V \text{ min.}} \times 100\%$$

   Measure the revolution from the counter.
   - The value of modulation is within 10%.

8. Move the head to track 00; press the Z key while running the RAM DATA test. Write 1F and measure the modulation. The value of modulation is within 10%.

9. Then, the inspection is completed.

IMPORTANT:

1. When the adjustment is made with the MODEL 100/TANDY 200, the dip switch position of the portable disk drive should remain as they are.

2. Be sure to remove the tape which covers the small cut of the encoder.

9. TROUBLESHOOTING

```
                    ┌─────────────┐
                    │    Start    │
                    └──────┬──────┘
                           │
              ┌────────────────────────┐
              │ Turn the power          │
              │ switch on and           │
              │ off                     │
              └────────────┬───────────┘
                           │
                     ╱───────────╲         YES
                    ╱ Is the       ╲──────────────────────┐
                    ╲ operation of  ╱                      │
                     ╲ initial track╱                       │
                      ╲ 0 normal?  ╱                        │
                       ╲─────────╱                          │
                           │ NO                             │
```

Start

Turn the power switch on and off

Is the operation of initial track 0 normal? — **YES** → Operation check with the host. / Check with exerciser (MODEL 100/ TANDY 200).

— **NO** →

Remove the upper case and turn the power on and off

Does feed mechanism function normally? — **NO** → Check the low battery lamp at the moment when the power switch is turned off

— **YES** →

Check the operation
1. Head carriage moves outward and hits the edge.
2. Head carriage moves inward and hits the edge.

1, 2 or 3

1 →

2 → TRK 0 sensor is normal or not.

3 → Does the stepping motor shaft rotate smoothly or not? — **NO** → Check the feed mechanism.

— **YES** →

Check the low battery lamp at the moment when the power switch is turned off

Does low battery lamp light in a moment? — **NO** → Fuse broken or not? — **YES** → Replace fuse. Power switch on

— **YES** →

Fuse broken or not? — **NO** → Check the power supply system.

Replace fuse. Power switch on → Fuse broken again? — **YES** → Check the power supply system.

— **NO** → To start.

Are the connector and lead wire of the stepping motor normal? — **NO** → Replace parts.

— **YES** → Check the PCBs.

— 55 —

10. PC BOARD VIEWS

Top View

Q102
P6
Q101
C105
DA102
R122
DA
101
DA103
R110
ZD
103
C120
R121
C113
C109
R142
P1
R W Y
VR101
C112 C111
C115
R138
L103
R137
L101
L102
DA
101 RA
R136 RA
R135 R134
R123
R124
RA102
(R101)
(SW101)
C118
R108
R109
ZD102
ZD 101
R117 R116 R115
R118
C106
C110
R114
X102
C108
R125 R127 R130 R133
R129 R126
R128
C119
C107
J5
LED 101
C104
R113
R141
R139
Q104
R112
C117
C116
R119 R131 R132 C114
DA104
P4
P3
P2
1 2 3 4 5 6 7 8 9
R120
#105
#108
#104
#103
#102
#101
#107
#106
85
86
(S)-708V
X101
C103
C102
ZD104
Q103
R140
R111
C101

Fig. 10-1

Bottom View

(5) Switch

(3) CH121

(2) CH120

(4) 0V

(1) CH102

(1) CH103

Fig. 10-2

11. EXPLODED VIEWS & PARTS LISTS

MECHANISM EXPLODED VIEW

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
39	Pad arm spring	ARB0507	W00101001
40	Screw, M2.6x4.6, with claw	AHD1047	W00471001
41	Screw 2.6, flat head	AHD1051	W00179001
42	Washer		W00198000
43	Snap ring E2	AHE0066	048020346
44	Binder #2		411746001
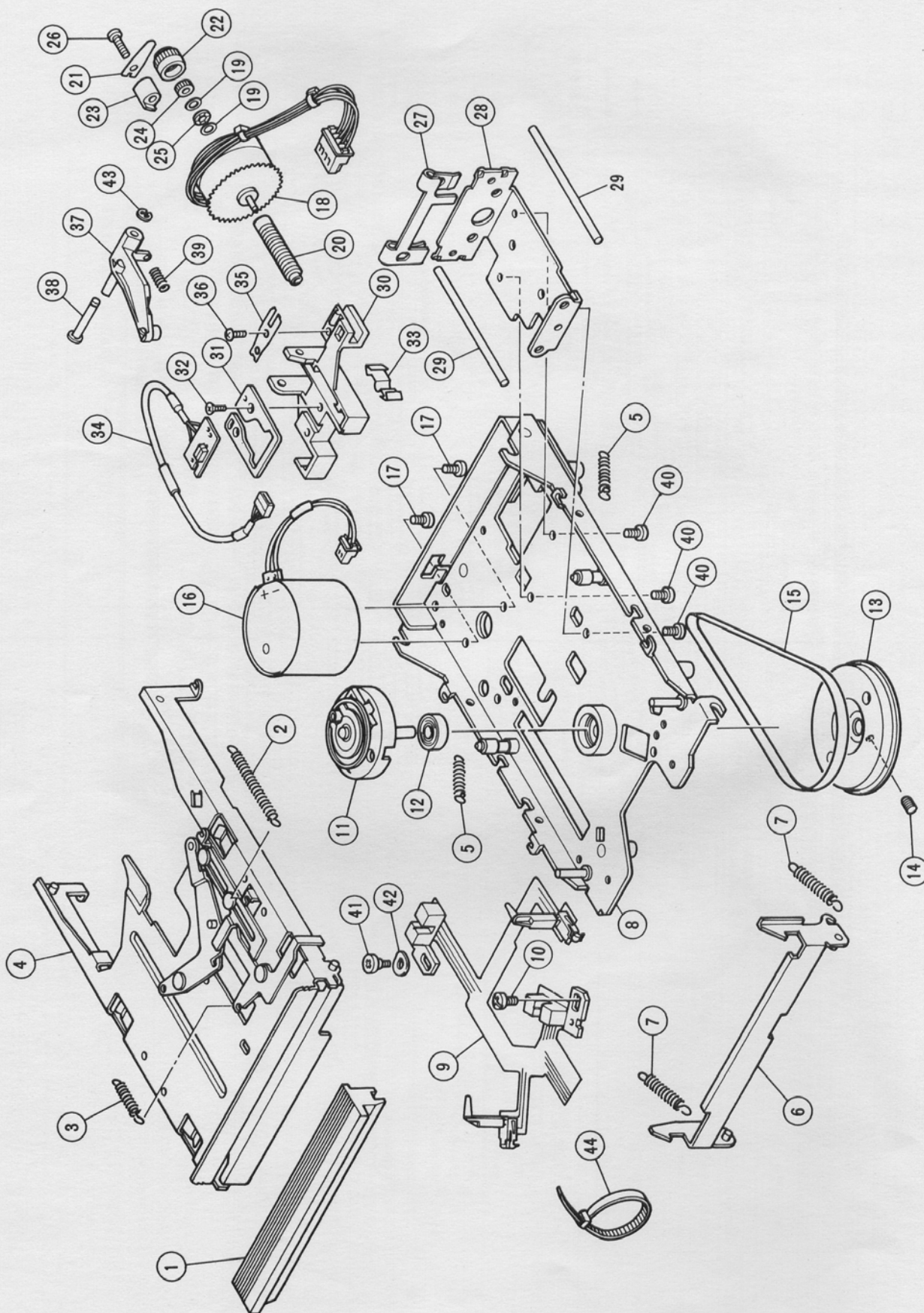
MECHANICAL PARTS

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
1	Disk in/out bar	ART0108	W00003002
2	Loading plate spring	ARB0500	W00004001
3	Loading nail spring	ARB0501	W00005001
4	Disk holder ass'y	ART0109	W00006001
5	Disk holder spring	ARB0502	W00017001
6	Clamp plate ass'y	ART0110	W00025001
7	Clamp spring	ARB0503	W00027001
8	Chassis ass'y		W00019001
9	Sensor cable ass'y	AW1025	W00028001
10	Screw, M3x4, binding head	AHD1045	060300406
11	Disk shaft ass'y	ART0111	W00031001
12	Ball bearing	AHC0121	W00041001
13	Disk pulley	ARA0029	W00042001
14	Set screw, M3x5, with hexagon socket	AHD1046	014300532
15	Urethan belt UR-70	AB6382	W00043001
16	DC motor ass'y, 0.6W	AM4010	W00044001
17	Screw, M2.6x4.6, with claw	AHD1047	W00471001
18	Step motor ass'y	AM4011	W00108001
19	Lead screw collar		W00048000
20	Lead screw		W00046401
21	SP holding plate spring	ARB0504	W00058001
22	SP cap	AHC0122	W00107000
23	Spacer	AHC0123	W00259000
24	Thrust collar	AHC0124	W00261000
25	Thrust ball bearing	AHC0125	W00264001
26	Screw, M26x10, pan head	AHD1048	062261006
27	Motor holding spring		W00055000
28	Motor holding plate		W00057001
29	Lead table shaft	ART0112	W00059001
30	Lead table ass'y	ART0113	W00060001
31	Head holder	ART0114	W00063000
32	Screw, M2x4, pan head	HD2007	061020406
33	Shaft holding plate spring	ARB0505	W00064000
34	Magnetic head ass'y with shield ring	AH4355	W80039001
35	Lead spring ass'y	ARB0506	W00065001
36	Screw, M2x3, truss head	AHD1049	008020316
37	Pad arm ass'y	ART0115	W00075001
38	Pad arm shaft ass'y	ART0116	W00109001

ELECTRONIC & ELECTRIC PARTS
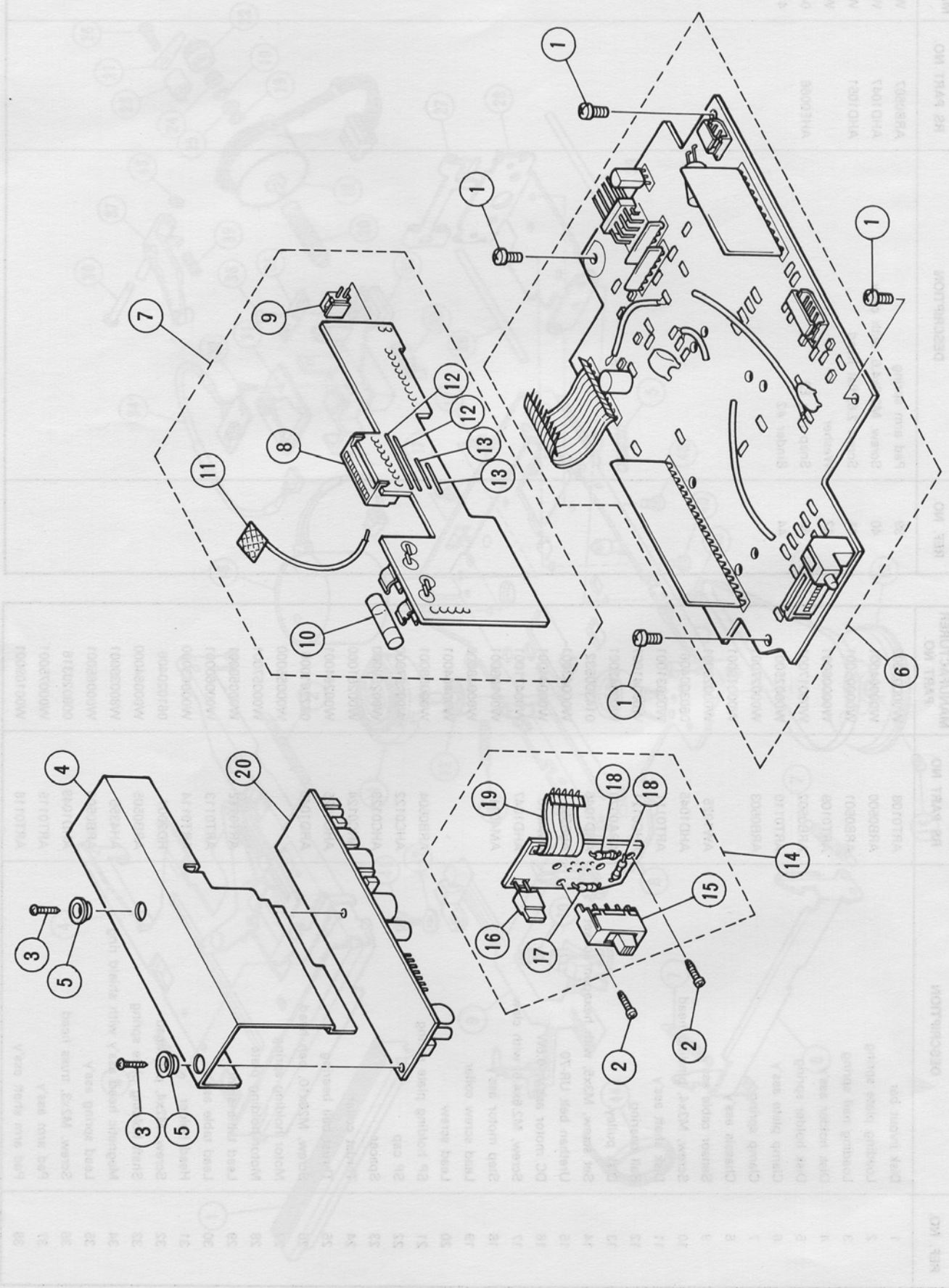
PCB INSTALLATION SECTION

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
1	Screw, M26x4, binding head	AHD1052	060260406
2	Screw, M2x6, pan head	HD2009	037200616
3	Screw, M2x8, pan head	HD2011	037200816
4	Upper shield plate assy		W00180001
5	Shield collar		W00181000

PCB ASSEMBLY

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
6	PCB, Main ass'y	AX3001	W00456001
	CAPACITORS		
C101	Capacitor, Ceramic, 0.1µF, +80%, −20%, 25V, GR42-6F104Z25PT	CC105ZFCP	W00142001
C102,103	Capacitor, Ceramic, 33pF, ±10%, 50V, GR42-6SL330K50PT	CC330KJCP	W00143001
C104	Capacitor, Ceramic, 0.1µF, +80%, −20%, 25V, GR42-6F104Z25PT	CC105ZFCP	W00142001
C105	Not used		
C106,107 C108	Capacitor, Ceramic, 0.1µF, +80%, −20%, 25V, GR42-6F104Z25PT	CC105ZFCP	W00142001
C109	Capacitor, Ceramic, 680pF, ±10%, 50V, GR42-6SL680K50PT	CC681KJCP	W00170001
C110	Capacitor, Ceramic, 33pF, ±10%, 50V, GR42-6SL330K50PT	CC330KJCP	W00143001
C111,112	Capacitor, Electrolytic, 10µF, ±20%, 16V, USA1C100MCA	CC106MDNP	W00145001
C113	Capacitor, Electrolytic, 100µF, ±20%, 6.3V, USA0J101MCA	CC107MBNP	W00146001
C114	Capacitor, Ceramic, 0.1µF, +80%, −20%, 25V, GR42-6F104Z25PT	CC105ZPCP	W00142001
C115	Capacitor, Ceramic, 2200pF, ±10%, 50V, GR42-6SL222K50PT	CC222KJCP	W00144001
C116,117	Capacitor, Ceramic, 0.1µF, +80%, −20%, 25V, GR42-6F104Z25PT	CC105ZFCP	W00142001
C118	Capacitor, Electrolytic, 100µF, ±20%, 16V	CC107MDAP	U51870000
C119,120	Capacitor, Ceramic, 0.1µF, +80%, −20%, 25V, GR42-6F104Z25PT	CC105ZFCP	W00142001

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
	CONNECTORS		
J5	Connector, 5597-09CPB	AJ1035	W00130001
J6	Connector, RF-H081SA-1114	AJ1036	W00856001
P1	Connector A4-4PA-2DS	AJ7011	W00356001
P2	Not used		
P3	Connector, 5268-02A	AJ1034	412412001
P4	Connector, 5268-04A	AJ1033	W00127001
	DIODES		
DA101,102 DA103,104	Diode 1SS226, Silicon	DX0375	W00122001
ZD104	Diode RD4.3MBI, Zener 4.3V	DX0376	W00123001
	ICs		
#101	LSI, HD63A01V1C22F, C-MOS 8bit CPU	MX5025	W00112001
#102	LSI, µPD65002G, C-MOS Gate array	MX5026	W00113001
#103	LSI, µPD449G, C-MOS 2KB S-RAM	MX5035	W00114001
#104	IC, TC50H000F, C-MOS Hex Buffer/Convertor Inveiting type	MX5036	W00115001
#105	IC, TC4584BF, C-MOS Shmitt Trigger Invertor	MX5037	W00116001
#106	IC, TC40H010F, C-MOS Triple 3-input NAND Gate	MX5042	W00117001
#107	HIC, MA7340, Read/Write Amp	MX5043	W00118001
#108	HIC, MA7339, Stepper driver	MX5044	W00119001
	RESISTORS		
RA101	Resistor array, RGSD3Y120J, Carbon, 120Ω, ¼W, 5%	ARX0032	W00126001
RA102	Resistor array, RGSD3Y103J, Carbon, 10KΩ, 0.25W, 5%	ARX	576247000
R108,109 R110,111	Resistor, MCR18-104EJ, metal, 100KΩ, ⅛W, 5%	ND0371EBE	W00132001
R112	Resistor, MCR18-564EJ, metal, 560KΩ, 0.125W, 5%	ND0429EBE	W00133001
R113	Resistor, MCR18-103EJ, metal, 10KΩ, 0.125W, 5%	ND0281EBE	W00134001
R114	Resistor, MCR18-105EJ, metal, 1MΩ, 0.125W, 5%	ND0445EBE	W00135001

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
	TRANSISTERS		
Q101	Transistor 2SC2712, NPN TR	2SC2712	W00120001
Q102	Transistor 2SA1286 PNP TR	2SA1286	U31504000
Q103,104	Transistor 2SC2712, NPN TR	2SC2712	W00120001
	MISCELLEANEOUS		
DS1	DIP switch 4P	AS1444	W00455001
JLW1	Jumper lead wire #1	AW1026	W00155001
JW101	Jumper wire 69		W00175001
JW102	Jumper wire 52		W00176001
JW103	Jumper wire 35		W00178001
JW104	Jumper wire 21		W00177001
L101,102 L103	Coil, 390µH, ±10%, LQN3N391K	ACA2021	W00147001
LA1	LED lamp ass'y	AL1012	W00150001
X101	Ceralock, CSA4.91MG	AC1180	W00124001
X102	Ceralock, CSA8.00MT	AC1181	W00125001
7	Sub PCB ass'y	AX3002	W00153001
8	Connector, 3024-08AH		W00156001
9	Connector, 5267-02A		U15266000
10	G fuse 1A TSC 1A	AHF0104	W00168001
11	Ground wire		W00159001
12	Jumper lead wire 20		W00172001
13	Jumper lead wire 10		W00173000
14	Panel PCB ass'y	AX3003	W00160001
15	Power switch, slide	AS1445	W00162001
16	LED (red) TLR208	AL1013	W00163001
17	Resistor, Carbon, 470, 0.25W, 5%	N0169EEC	090471120
18	Resistor, Carbon, 100, 0.25W, 5%	N0132EEC	090101120
19	Jumper lead wire #2	AW1027	W00158011
20	DC-DC converter	AX3004	W00167001

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
R115,116 R117,118	Resistor, MCR18-104EJ, metal, 100KΩ, 1/8W, 5%	ND0371EBE	W00132001
R119	Resistor, MCR18-272EJ, metal, 2.7KΩ, 0.125W, 5%	ND0224EBE	W00136001
R120	Resistor, MCR18-391EJ, metal, 390Ω, 0.125W, 5%	ND0162EBE	W00454001
R121,122	Resistor, MCR18-472EJ, metal, 4.7KΩ, 0.125W, 5%	ND0247EBE	W00138001
R123	Resistor, MCR18-272EJ, metal, 2.7KΩ, 0.125W, 5%	ND0224EBE	W00136001
R124	Resistor, MCR18-472EJ, metal, 4.7KΩ, 0.125W, 5%	ND0247EBE	W00138001
R125	Resistor, MCR18-333EJ, metal, 33KΩ, 0.125W, 5%	ND0324EBE	W00139001
R126	Resistor, MCR18-471EJ, metal, 470Ω, 0.125W, 5%	ND0169EBE	W00137001
R127	Resistor, MCR18-333EJ, metal, 33KΩ, 0.125W, 5%	ND0324EBE	W00139001
R128	Resistor, MCR18-471EJ, metal, 470Ω, 0.125W, 5%	ND0169EBE	W00137001
R129,130	Resistor, MCR18-103EJ, metal, 10KΩ, 0.125W, 5%	ND0281EBE	W00134001
R131,132	Resistor, MCR18-104EJ, metal, 100KΩ, 1/8W, 5%	ND0371EBE	W00132001
R133	Resistor, MCR18-471EJ, metal, 470Ω, 0.125W, 5%	ND0169EBE	W00137001
R134,135 R136	Resistor, MCR18-103EJ, metal, 10KΩ, 0.125W, 5%	ND0281EBE	W00134001
R137	Resistor, MCR18-681EJ, metal, 680Ω, 0.125W, 5%	ND0183EBE	W00140001
R138	Resistor, MCR18-103EJ, metal, 10KΩ, 0.125W, 5%	ND0281EBE	W00134001
R139	Resistor, MCR18-472EJ, metal, 4.7KΩ, 0.125W, 5%	ND0247EBE	W00138001
R140	Resistor, MCR18-471EJ, metal, 470Ω, 0.125W, 5%	ND0169EBE	W00137001
R141	Resistor, MCR18-104EJ, metal, 100KΩ, 1/8W, 5%	ND0371EBE	W00132001
R142	Resistor, MCR18-472EJ, metal, 4.7KΩ, 0.125W, 5%	ND0247EBE	W00138001
VR101	Resistor, Semi-fixed, RVG0707H100-10-303M	Ap6007	W00141001

HOUSING PARTS

HOUSING PARTS

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
1	Front bezel ass'y		W00297001
2	Front bezel	AZ3958	W00298001
3	Washer A type		W00349000
4	Eject button	AK0347	W00084002
5	Upper case ass'y	AZ3959	W00085002
6	Lower case ass'y	AZ3960	W80003001
7	Battery case cover	ADB0261	W00090002
8	Dip switch cover	AHC0126	W00091002
9	Battery coil spring	AB0625	W00095001
10	Battery contact ass'y	AB0626	W00102001
11	Switch sheet		W00099001
12	Power switch cover	AHC0128	W00100002
13	Screw, M3x16, pan head	HD2066	062301606
14	Lower shield plate ass'y		W00182001

ACCESSORIES
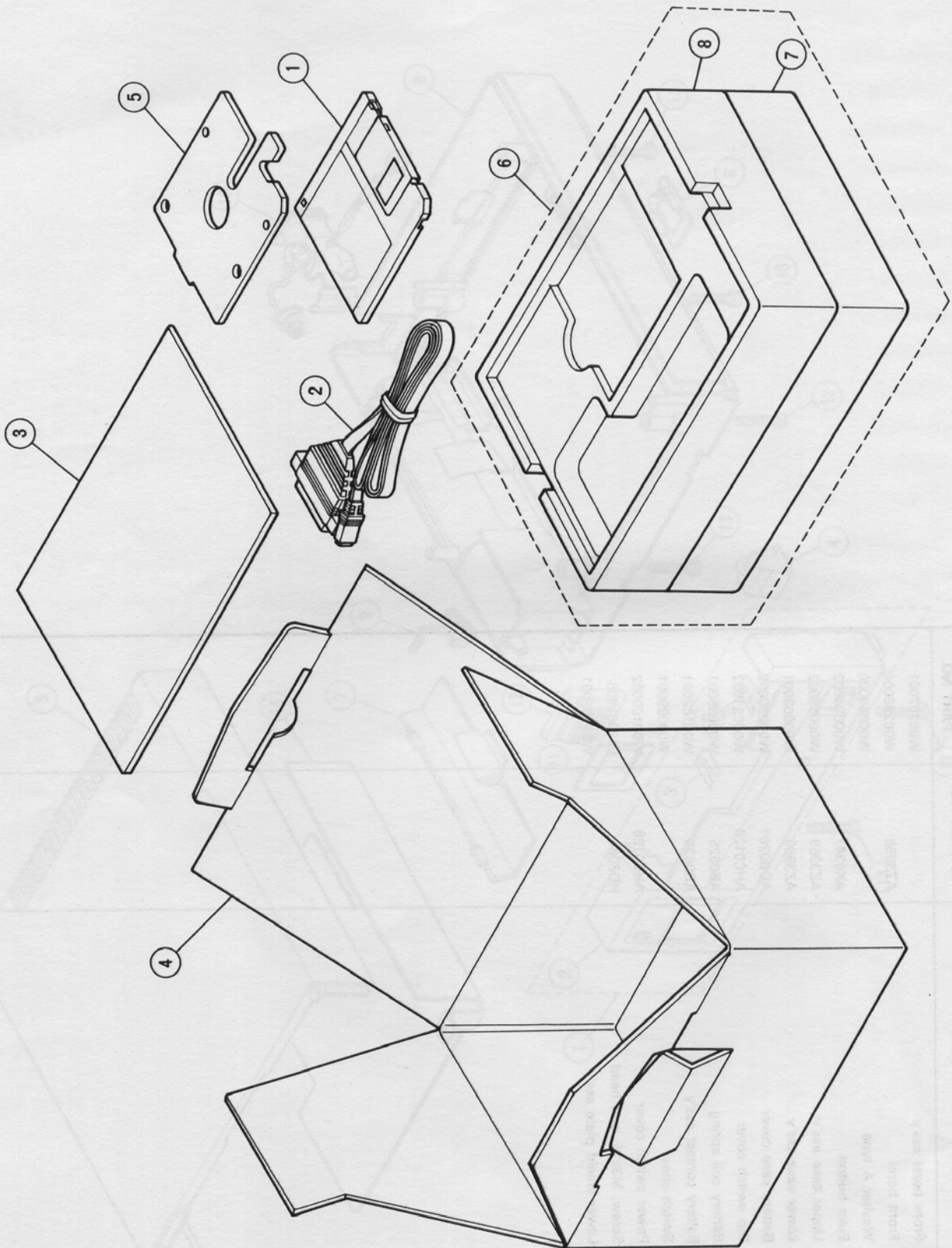
ACCESSORIES

REF. NO.	DESCRIPTION	RS PART NO.	MANUFACTURER PART NO.
1	Utility diskette	AXX2029	W0045800
2	Serial cable	AW1028	W0045700
3	Owner's manual	MU2603808	W91110011
4	Individual carton		W60011001
5	Head protect sheet	AHC0127	W0046300
6	Polystyrene form assy		W60012000
7	Lower polystyrene form		W60014000
8	Upper polystyrene form		W60013000

12. SCHEMATIC DIAGRAMS
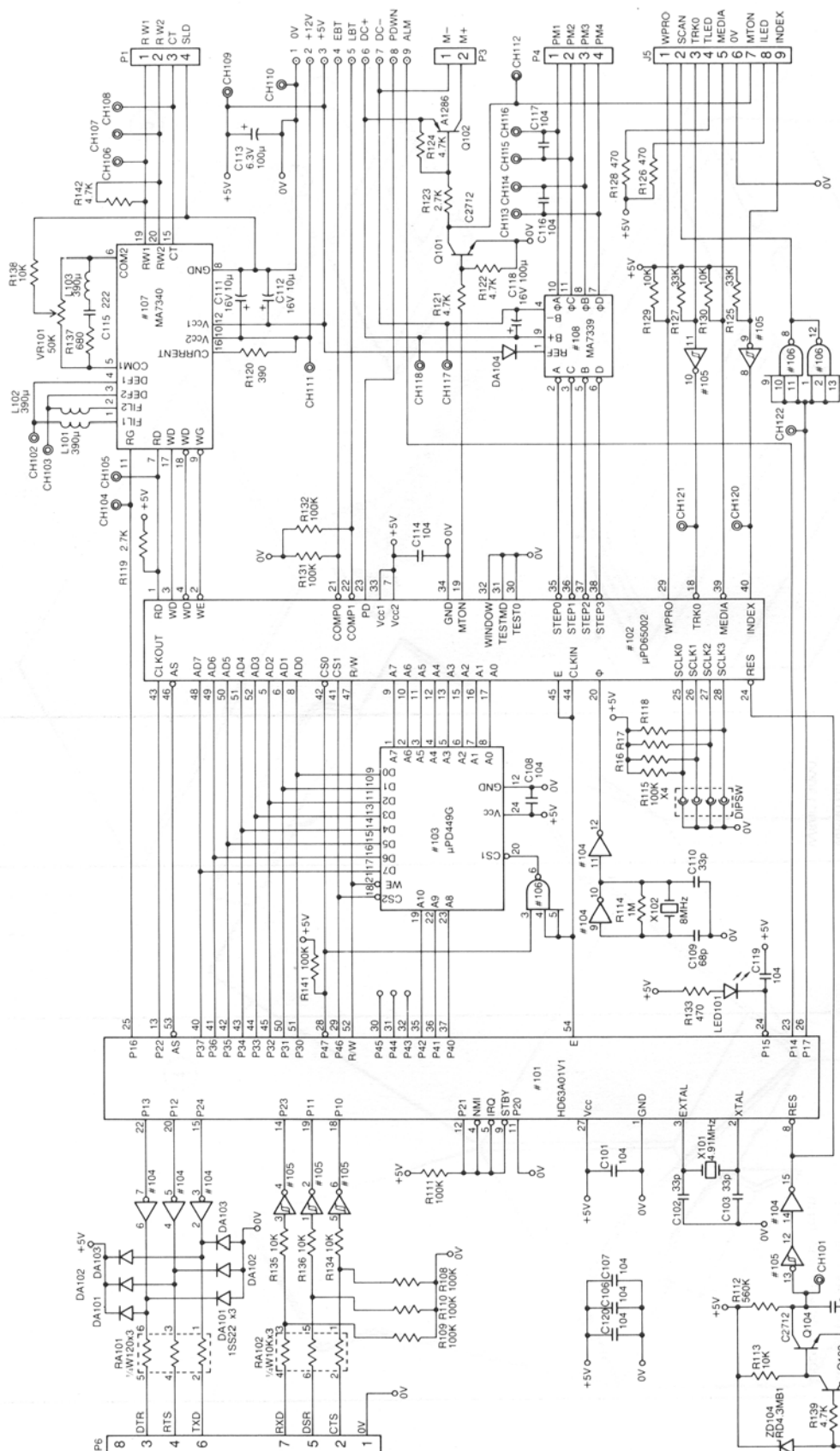
NOTES:
A) RATED POWER OF UNSPECIFIED RESISTOR: 1/8W
B) #104: TC50H000F, #105: TC4584F, #106: TC40H010F
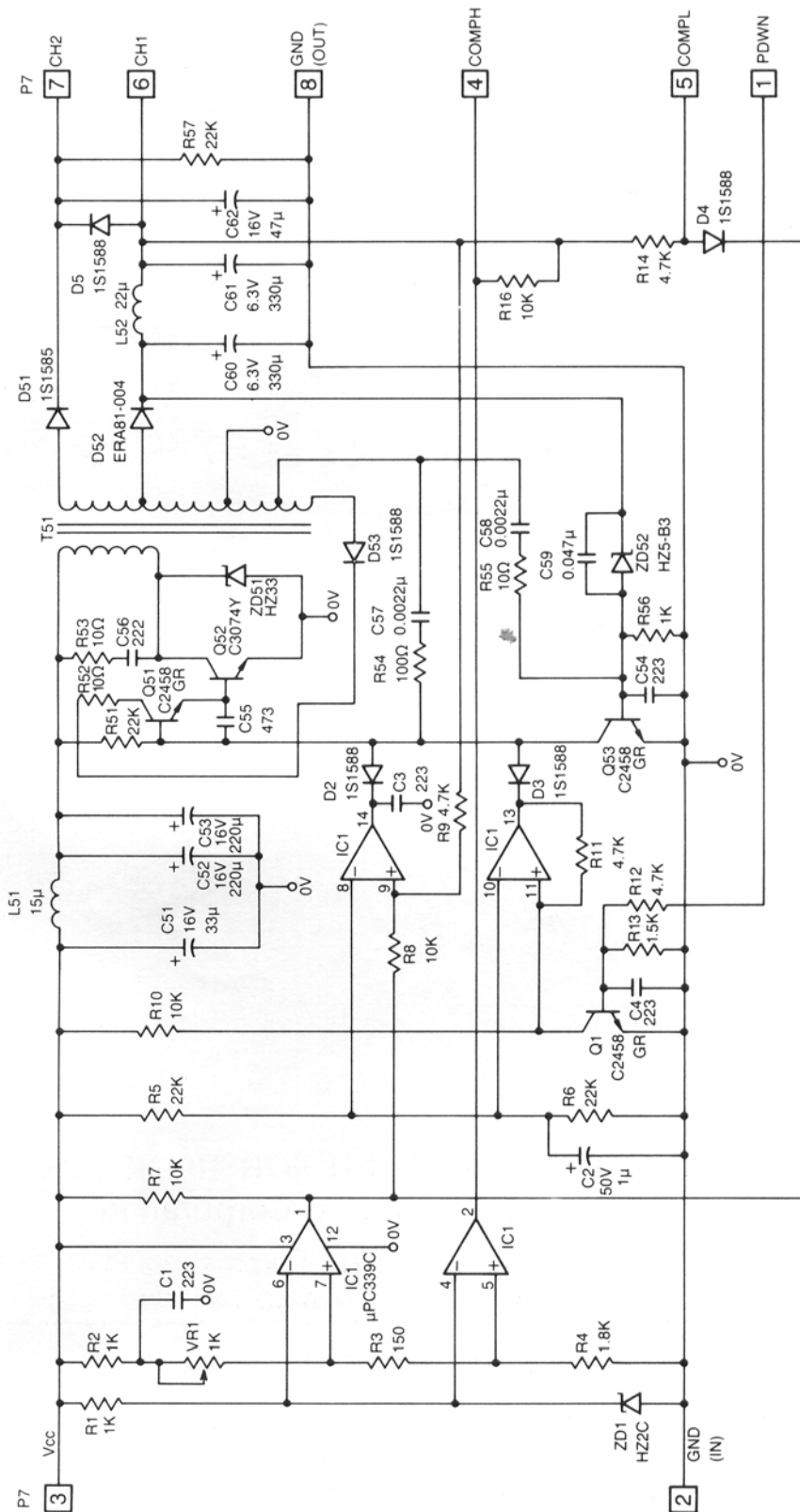
Fig. 12-1. Schematic Diagram of Main PCB

Fig. 12-2 Schematic Diagram of DC-DC Unit